

# **NANO-FET DEVICES:**

MINIATURIZATION, SIMULATION,  
AND APPLICATIONS - PART 2

Editors:

**Dharmendra Singh Yadav  
Prabhat Singh**

**Bentham Books**

**Nano-FET Devices:  
Miniaturization, Simulation, and  
Applications**  
*(Part 2)*

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## **Nano-FET Devices: Miniaturization, Simulation, and Applications (*Part 2*)**

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## FOREWORD

Welcome to the world of Nano-FET Devices, where innovation meets the frontier of miniaturization. The evolution from traditional MOSFETs to nanoscale transistors—such as Single Electron Transistors, Carbon Nanotube FETs, Nanowire FETs, and Graphene FETs—has marked a significant leap in semiconductor technology. These advancements have not only enhanced performance and energy efficiency but also expanded applications into areas like biosensing and biomedical engineering. As the demand for faster, smaller, and more efficient devices continues to grow, Nano-FETs have emerged as key enablers of next-generation electronics. Their unique properties offer superior control at the atomic scale, making them ideal for applications ranging from ultra-low-power systems to high-frequency communication.

This book provides a focused exploration of Nano-FET devices—covering their operating principles, simulation techniques, and diverse applications. Emphasis is placed on simulation methodologies, including quantum mechanical and device-level modeling, which are essential for accurate performance prediction and design optimization. With practical insights, real-world examples, and a strong foundation in theory, this book bridges the gap between research and application. It is intended for researchers, engineers, and students eager to explore the transformative potential of Nano-FET technology.

We invite you to begin this journey into the future of electronics—where quantum effects, novel materials, and nanoscale engineering converge to shape tomorrow's devices.

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## PREFACE

Millions of transistors comprise an integrated circuit. Transistors are the essential aspect of all modern electrical components and electronic devices. The size of the transistors has been progressively shrunk as the VLSI industry grows to integrate more functionality onto a silicon wafer and minimize circuit power consumption. Nano-FET devices are being realized using various materials with different structures, with promising results. Novel nano-FET devices should be an excellent candidate to replace the existing technologies for low-power and high-frequency applications with reduced time delay in circuit applications.

The relentless pursuit of miniaturization in semiconductor technology has led to the emergence of nano FETs as pivotal components in modern electronic systems. This book aims to provide a comprehensive overview of nano FET devices, from their theoretical foundations to application implementations. Due to the enormous study of Nano-CMOS and post-CMOS technologies and the lack of a comprehensive guidebook, research articles are now the cornerstone for the knowledge of novel design based on the fundamentals of Nano-FET devices. As a result, this book outlining the essential characteristics of Nano-CMOS and post-CMOS technologies will benefit engineers who must understand the fundamentals of these devices and scholars developing/implementing Nano-CMOS and post-CMOS devices and their applications. This book, *Nano-FET Devices: Miniaturization, Simulation, and Applications*, is intended to fulfill this requirement of the research community.

In the opening chapters, readers will embark on a journey through the basic concepts of FETs, understanding how these devices operate and their significance in electronic engineering. Building upon this foundation, the book delves into the unique characteristics of nano FETs, including quantum effects, scaling considerations, and material properties that define their behavior at the nanoscale.

This book is a concise benchmark for beginners who are just getting started with Nano-FET Devices and their application with recent advancements, and those who want to design integrated circuits using novel FET devices. We hope that "*Nano-FET Devices: Miniaturization, Simulation, and Applications*" serves as a valuable resource for researchers, engineers, and students interested in unlocking the potential of nano-FET technology. May this book inspire discoveries, innovations, and advancements at the forefront of electronic engineering.

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## **DEDICATION**

I would like to dedicate and express my hearty gratitude towards my respected parents, Uncle, aunty, younger brothers, sisters for their affection and persistent efforts in my education. Also dedicated to my wife and our loving son Armaan Singh for their everlasting supports, encouragements and understanding. This work is dedicated to my family and others who have always been as source of my continued efforts for academic excellence. Over to all infinite gratitude flows to the almighty for the countless blessings bestowed upon us.

— **Dharmendra Singh Yadav**

I dedicate this book to my loving mother, Shakuntala Singh, my father, Dinesh Singh, my wife, Sadhana Singh, and my brother, Prasoon Singh, as a token of deep appreciation for everything you have done and continue to do for me. Your love and support are the foundation of my success, and I am truly blessed to have you in my life. I also wish to dedicate this book to Dr. Nagendra Pratap Singh, Dr. Ashish Raman, and Dr. Navjeet Bagga for their invaluable guidance and unconditional support, which have played a crucial role in helping me achieve this success. This book is a symbol of my heartfelt gratitude for all that you have done.

— **Dr. Prabhat Singh**

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**CHAPTER 1****Physics and Properties of Single/ Multi-Gate Fets****Subarna Mondal<sup>1,\*</sup>, Soumya Sen<sup>2</sup> and Ashish Raman<sup>3</sup>**<sup>1</sup> *ECE Department, Maulana Abul Kalam Azad University and Technology, West Bengal, India*<sup>2</sup> *Computer Science and Engineering Department, University of Engineering and Management, Jaipur, Rajasthan, India*<sup>3</sup> *ECE Department, B. R. Ambedkar National Institute of Technology, Jalandhar, Punjab, India*

**Abstract:** In the semiconductor industry, the integration of the Complementary-Metal-Oxide-Semiconductor (CMOS) mechanism into Integrated Circuits (ICs) has resulted in a significant rise in the count of transistors on a single chip. This is made possible by shrinking down the size of Metal-Oxide-Semiconductor-Field-Effect-Transistors (MOSFETs). However, scaling can lead to device performance degradation. To address this, advanced MOSFET designs like multi-gate transistors, junction-less transistors, and Tunnel FETs have been proposed, aiming to sustain Moore's Law and support continued transistor scaling in the coming decade. The key principles of this chapter involved in both single and multi-gate FETs include quantum mechanics, carrier transport, and electrostatics. The scaling of transistors to smaller sizes involves considerations of quantum effects, like tunneling and quantum confinement, which have a significant impact on their behavior. Understanding this chapter is crucial for optimizing their performance, enabling further miniaturization, and enhancing the capabilities of integrated circuits. Additionally, it plays a crucial role in advancing the field of next-generation electronics and computational devices.

**Keywords:** Electrostatic integrity, Quantum mechanics, Quantum confinement MOSFET, FET, multi-gate FET, Single gate FET.

**INTRODUCTION**

The advancement of semiconductor technology has been a relentless march to make more capable and efficient electronic devices. A pivotal chapter in this technological journey is the transition from single-gate Field-Effect Transistors (FETs) to multi-gate FETs, a transformation that has redefined the boundaries of modern electronics. This journey reflects not only a remarkable evolution in

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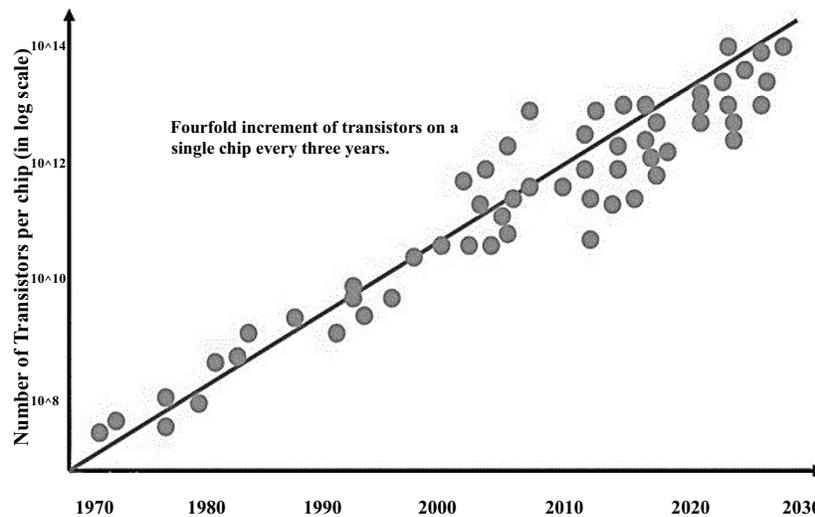
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transistor design but also a testament to human ingenuity and the relentless pursuit of greater computing power. Single-gate FETs, such as the well-known Metal-Oxide-Semiconductor FETs (MOSFETs), have been the linchpin of electronics for decades. They served as the foundational element for integrated circuits and electronic systems by utilizing a lone gate electrode to regulate the current between the source and drain terminals. Yet, as the demands for more compact and energy-efficient devices grew, it became evident that single-gate FETs were approaching their performance limits. The shift towards multi-gate FETs represents a transformative leap in semiconductor technology [1-3]. Multi-gate FETs, also known as multi-gate transistors, feature multiple gate electrodes, enabling enhanced control over the flow of electrons within the channel. The most prominent of these innovations is the FinFET (Fin Field-Effect Transistor), which utilizes a three-dimensional fin-shaped channel and multiple gates to govern the electron flow [4]. This design innovation has set the stage for unprecedented scaling and performance improvements. The progression from single to multi-gate FETs began in response to the semiconductor industry's challenge of maintaining Moore's Law [3]. Renowned for his observation, Intel co-founder Moore noted that the number of transistors on a microchip would undergo a doubling roughly every two years [2], leading to exponential advancements in computing power. However, as transistor dimensions approached the nanoscale, the limitations of single-gate FETs became increasingly apparent. Issues such as leakage current, power consumption, and heat dissipation threatened to stall the progression of Moore's Law [4]. Section 2 focuses on the evolution of FET technology and recalls the history of the single to multi-gate concept. It also highlights the benefits of multi-gate FETs in terms of precise control over short channel effects. Section 3 discusses the basic physics of single-gate FET to multi-gate FET and also analyzes the electrostatics of the multi-gate MOS system. The study also investigates the influence of electron excavating through narrow gate dielectric. Section 4 introduces a different structural view of multi-gate FET in Silvaco atlas TCAD, its working,  $I_d$ - $V_d$  characteristics, and Ion-Ioff ratio. Section 5 discusses the profound impact of multi-gate FET in nanotechnology by enabling improved performance, energy efficiency, continued scaling, and sustenance of Moore's law. Section 6 focuses on challenges in simulating Multi-gate FET and structural analysis hurdles and reviews structural modification to address this issue.

## **PROGRESSION OF FET TECHNOLOGY**

In 1965, Gordon Moore's influential paper foresaw a fourfold increase in transistors on a single chip every three years, laying the groundwork for Moore's Law [2]. The semiconductor industry has closely adhered to this law, with collaborative efforts

between semiconductor firms and educational institutions working towards refining the accuracy of industry predictions since the early 1990s. This collaboration led to the establishment of the International Technology Roadmap for Semiconductors (ITRS) organization [5]. The ITRS releases an annual outline, serving as a reference for the semiconductor sector, outlining the required technology, tools for design, and equipment to match the swift advancements in semiconductor devices projected by Moore's Law (Fig. 1).



**Fig. (1).** This picture illustrating the number of transistor vs years according to Moore's theory [5].

Silicon CMOS is the essential technology at the core of the semiconductor industry, and the MOS transistor, also known as the MOSFET (MOS Field-Effect Transistor), stands as its cornerstone. To align with the relentless progression defined by Moore's Law, the physical measurements of transistors have consistently undergone a halving every triennial. The challenge of sub-micron scale dimensions was effectively addressed in the early 1980s. Looking back to 2023, the semiconductor industry considered the introduction of 3nm and 5nm nodes to achieve greater transistor density and performance. These technological strides will empower the development of processors, memory modules, and System-on-Chip (SoC) designs.

The physics of single to multi-gate-field effect transistors (FETs) is a fundamental aspect of modern semiconductor technology. The concept of multi-gate-Field-Effect-Transistors (Mug-FETs), namely double, triple, and quadruple gate SOI MOSFET, has emerged as a favorable choice to align with the scaling trends

## Emerging and Future Prospective of Carbon Nanotube FETs

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**Abstract:** In the last few years, the semiconductor industry has brought about a drastic revolution in the existing technology in order to realize a larger on-chip integration, enhance performance, increase operating speed, and decrease energy consumption. Delay and power consumption have become the most vital performance parameters of any digital circuit. One of the methods devised to achieve this is by scaling the feature size of a transistor. However, when the channel length is reduced beyond 45nm in metal-oxide-semiconductor field-effect transistors (MOSFETs) technology, it gives rise to perilous complications and challenges such as decreased gate control, short channel effect, increased power density, higher sensitivity to process deviation, higher manufacturing cost, and increased leakage current. This draws a limit on the transistor size and demands for new transistor structures and technologies to overcome the drawbacks. Technologies like benzene rings, single electron transistors (SET), Quantum-dot cellular automata (QCA), and carbon nanotubes are slowly rising as alternatives to reduce the problems associated with CMOS. New technologies demand faster processors, smaller sizes, and less power consumption. Advances in 5G networks have increased the pressure to improve the battery life of smartphones, their performance, spectral efficiency, and many more. The potential to achieve these is the use of Carbon Nanotube Field Effect Transistors (CNTFETs). They have higher carrier mobilities and direct band gaps that enhance the band-to-band tunneling and optical properties. These features make CNTFETs suitable to be used in future novel electronic devices. Hence, this chapter focuses on the emerging and future trends of CNTFETs. The constructional aspects, features, types, designs, and applications of CNTFETs are dealt with in detail in the forthcoming sections of the chapter.

**Keywords:** CNTFET, CNTs, Chiral vectors, Dielectric materials, High K dielectrics, Short channel effects.

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## **INTRODUCTION**

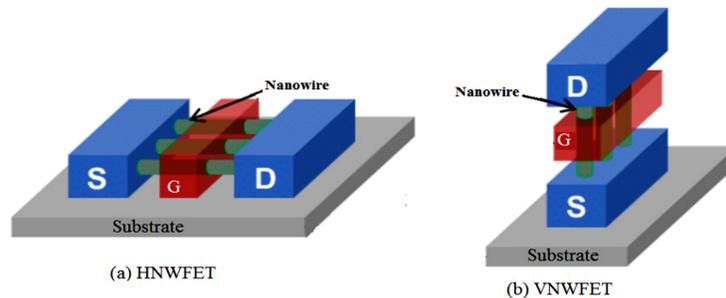
The consistent scaling of both active and passive electronic components that are unified on ICs has paved the way for an exponential growth of silicon-based microelectronics in the last few decades. Scaling of the feature size has reduced the size of the transistor, decreased the burden on testing, reduced the cost, and has made the switching faster, in addition to other advantages like low power and reliable designs. The growth is in accordance with Moore's law, which says that the integration of transistors on a chip doubles every 18 months [1].

At present, the technology node has reached a scale of 14nm, and further scaling down the channel length will lead to critical short-channel effects and reliability issues. Increment in the metallic on-chip interconnects, and power dissipation also makes the MOSFETs unsuitable for advanced applications. To overcome the short-channel effects of traditional MOSFETs, double-gate MOSFETs and FINFETs have emerged. In such devices, the gate is placed on two or three sides of the channel in order to establish higher control over the channel. The arrangement also brings about a considerable decrease in the leakage current that exists between the drain and the source [2, 3].

Propagation delay, area, cost, and reliability are the main concerns at present for VLSI design engineers. With the increased usage of portable devices like mobile and laptops, lower energy-consuming devices are in huge demand. As compared to microelectronic technology, developments in battery technology are slower. The situation has been further worsened by the fact that the clock speed of the microprocessor has reached the GHz limit, which paves the way to increased energy consumption. Hence, there is a requirement to develop VLSI circuits to reduce power dissipation, and in the near future, the technology, however, is expected to drift from conventional silicon-based MOSFETs and FINFETs to Nanowire Field Effect Transistor (NWFET) [1], Graphene Field Effect Transistor (GFET), and Carbon Nanotube Field Effect Transistor (CNTFET), owing to the critical issues faced by FINFETs like the difficulty in manufacturing thin fins and controllability of the channel in advanced nodes [4].

NWFET is a device in which the channel is surrounded by a gate all around and a semiconducting nanowire of diameter about 0.5nm is used as channel material. The nanowire may be made with Si, SiC, germanium, and ZnO semiconductors. The tiny diameter of the nanowire helps in reducing the short channel effects, as well as in 1-D conduction. NWFET has the potential to replace MOSFET owing to its improved performance and low power when the technology nodes are to be scaled

beyond 7nm. NWFETs can be designed both horizontally (H-NWFET) and vertically (V-NWFET), as depicted in Fig. (1). The circuit design of H-NWFET is similar to that of FINFET. This feature makes it a potential candidate to replace FINFET. In contrast, V-NWFET has a radical design style and occupies a small area.



**Fig. (1).** H-NWFET and V-NWFET structures [6].

However, the challenge faced by the device is in the diffused PN junction fabrication. Although a metal drain-source junction is used, it still faces problems with a large off-state current.

2D materials have the advantages of being small in size and having low cost and mass fabrication capacity. They also have excellent mechanical strength and are highly flexible; hence, they have become promising blocks for many devices. Graphene is a classic example of a 2D material.

The graphene field effect transistor consists of a source, drain, and top or back gate as a MOSFET, as depicted in Fig. (2). But unlike the MOSFET structure, it has a thin graphene channel between the source and drain, which is usually tens of microns thick. Graphene is usually found as a single carbon atom layer material that is tightly packed in a 2-D honeycomb hexagonal lattice. Graphene offers superior electrical properties, higher thermal conductivity, good optical properties, and excellent chemical properties. It has the capacity to deliver 100 to 1000 times better performance than Si-based MOSFET. Despite advantages, graphene-based FETs have setbacks like low on-off current ratio, no bandgap, which makes it work as a metal, and insufficient saturating current that stops the device from attaining maximum voltage gain and oscillation frequency in Radio Frequency (RF) applications [7, 8].

**CHAPTER 3****The Future Outlook for Field Effect Transistors Using Carbon Nanotubes****C. Kathiravan<sup>1,\*</sup>, Gowrishankar J.<sup>2</sup>, S. Grace Infantiya<sup>3</sup>, D. Anbuselvi<sup>3</sup> and N. Suthanthira Vanitha<sup>4</sup>**<sup>1</sup>*Department of Chemistry, Muthayammal Engineering College, Rasipuram, Namakkal, India*<sup>2</sup>*Department of Computer Science and Engineering (AI) JAIN (Deemed-To-Be University), Bangalore, India*<sup>3</sup>*Department of Physics, Muthayammal Engineering College, Rasipuram, Namakkal, India*<sup>4</sup>*Department of Electrical and Electronics Engineering, Muthayammal Engineering College, Rasipuram, Namakkal, India*

**Abstract:** Carbon Nanotube Field Effect Transistors (CNTFETs) are potential nano-scaled devices for realising high-performance, very dense, and low-power circuits. A Carbon Nanotube Field Effect Transistor is a FET that uses a single CNT or an array of CNTs as the channel material rather than bulk silicon as in a standard MOSFET configuration. A carbon nanotube is at the heart of a CNTFET. This paper provides an overview of CNTFETs-pH sensor based on carbon nanotubes (CNTs)-FETs-pH measurement range of 1.34 to 12.68, reliability, and low hysteresis, indicating a promising application prospect in harsher testing environments. The determination of carbamate pesticides-adjusting the  $V_{TH}$  revealed that carbaryl and carbofuran additions had a favorable effect on the CFO/s-SWCNT-FET and structure. In this chapter, modeling, fabrication, and applications have been discussed devices.

**Keywords:** Carbon nanotubes or Buckytube, FET-Uni-polar transistors, nanoelectronics, pH sensors, environmental stability, s-SWCNTs, CFO/s-SWCNT.

**INTRODUCTION**

Integrated circuits are widely used in our daily lives, especially personal computers and mobile gadgets. As economic conditions and electronic technology advance, people demand more powerful and lighter gadgets [1]. Carbon Nanotube Field Effect Transistors (CNTFETs) or Carbon Nanotube Uni-polar transistors hold

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significant promise as a nanoscale technology for developing densely packed, low-power, high-performance circuits. A CNT-Uni-polar transistor is a semiconductor device that, unlike MOSFETs, typically uses bulk silicon as the channel material that is used in carbon nanotubes [2-10].

A carbon nanotube forms the core of a CNTFET. Uni-polar transistor biosensors have sparked considerable attention due to their unique high sensitivity. Traditional Uni-polar transistor (FET) biosensors often lack stability due to the intricate connection between the sample solution and the transistor. The harsh acidic or basic conditions in which they operate can lead to connection failures in Uni-polar transistor-based pH sensors, making it difficult to monitor pH consistently, correctly, and with low hysteresis, we present a pH sensor based on carbon nanotubes (CNTs)-FETs that have better environmental stability due to the addition of a HfO<sub>2</sub> layer to the gate insulator. The proposed technologies exhibit the necessary resistance to external influences, including a wide range of chemical and sensible constituents. Mostly, we demonstrated that this CNT-FET device could be utilized to continuously detect pH. It has 68 mV / pH sensitivity, a pH value of 1.0 -13, a minimal hysteresis of 600 pA, and pH altering loops of 4-10 [11-15].

Because of their distinctive geometries with high surface-to-volume and aspect ratios, Buckytube Uni-polar transistors, in particular, with single-wall carbon nanotube connecting channels, present exciting possibilities for very sensitive and label-free biosensors and chemical sensors [16-25]. SWNTs have all of their atoms on the surface and are accessible to the environment. As a result, even small shifts in the charge environment may significantly change their electrical properties [2]. Unipolar transistors based on semiconducting single-walled carbon nanotubes have demonstrated several advantages, including high transporter ability to adapt, either high on or high off ratio, electron transport that is semi-ballistic, name-free discovery, and steady reaction. Thus, cobalt ferrite oxide (CFO) nanoparticle-adorned s-SWCNTs were arranged and employed to connect the source and channel cathodes. For non-enzymatic carbaryl and carbofuran recognition, cobalt ferrite oxide /s-SWCNT/FET was used as planned. When used as a detection stage, the cobalt ferrite oxide /s-SWCNT half-breed film demonstrated great responsiveness and selectivity with the least restriction of discoveries for the compound like carbaryl and carbofuran (0.10fM) and (0.067fM) respectively, and a broad direct range of location from 10 to 100fM respectively. Moreover, this sensor was utilized to distinguish between carbaryl in experiments on tomatoes and cabbage, validating its accurate identification. The charge move response on the s-SWBTs/FET conduction channels progressed as a result of the execution, which may be attributable to the forceful synergist movement of CFO oxidizing carbamate. The

sophisticated CFO/s-SWCNT-based detection methodology described in this paper may be applied to assess pesticide residues in food testing [26-37].

Traditional silicon-based complementary metal oxide semiconductor devices are approaching their basic scalability restrictions. This has prompted a lot of interest among researchers in looking into cutting-edge device technologies that use diverse materials to keep the scaling boundaries of modern integrated circuits. Carbon nanotubes have been extensively researched as a prominent material alternative across various fields due to their advantageous properties such as reduced short channel effects, high mobility, and high normalized driving currents. CNTs make up the majority of carbon nanotube Uni-polar transistors, which are regarded to be the most practicable alternatives to silicon transistors [38-40].

## **CARBON NANOTUBE FIELD-EFFECT TRANSISTOR**

MOSFETs of today are comparable to carbon nanotube Uni-polar transistors. The source, drain, and gate are the three terminals they need. The current flow at the drain terminal and source is regulated by the gate. Current can pass via a channel and across the source when the gate is activated. The use of carbon nanotubes as the channel in CNFETs versus heavily doped silicon in MOSFETs is the primary difference between the two types of transistors. Complementary devices, such as semiconductors, are essential to both technologies. They are reliable, boost gain, use less power, and integrate readily into logic circuits. Holes are conducted via a p-type transistor and an n-type transistor carries electrons. Both sorts, as well as another type of device, will be investigated, with an emphasis on their production and swapping.

### **Current CNFET Designs' Blueprint**

#### ***Development***

Because the goals of these devices were essentially proof of concept and rudimentary comprehension, the first CNFETs were constructed in the most basic manner imaginable. Fig. (1) [3] shows first-generation CNFETs. The source and drain are represented by the two gold electrodes over which the nanotube is wrapped. It is possible to place the gate underneath or to the side of the transistor. Moreover, an insulator, like silicon dioxide, separates the gate from the nanotube. The electric field can be used to switch on and off the transistor because the gate is isolated. The transistor would become unusable if it was not protected from short circuits.

## Advancements in Nanomaterial Integration for Enhanced Biosensing Applications: Focus on Field Effect Transistor (FET)-Based Devices

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**Abstract:** The accelerating advancement of nanoscience and nanotechnology has established an explosion of potential opportunities for the fabrication of miniaturized nanostructured components with specialized applications in biology, electronics, chemistry, mechanics, and computational functions. This has a huge impact on the special field of biosensors, empowering the fabrication of extremely sensitive, compact, and effective diagnostic equipment. Notably, among these aforementioned advances, the nano-based Field-Effect Transistor (NFET) serves as an attractive candidate for biosensor applications owing to its remarkable attributes, including label-free detection, a high level of sensitivity, rapid response times, continuous measurement capabilities, low consumption of electricity, and potential for miniaturization into compact devices. Each of these traits combines to make nano-based FET biosensors, an interesting and robust technology for a variety of biomedical applications. In recent years, the integration of semiconducting materials, polymers, and carbon-based biocompatible nanomaterials has significantly revolutionized biosensing applications. These materials have been strategically incorporated into various nanostructures to elevate the efficacy and sensitivity of biosensing devices, particularly in the realm of field-effect transistor (FET)-based systems. This proposed book chapter aims to explore the burgeoning landscape of biocompatible nanomaterials and their role in the evolution of biosensing technologies. The utilization of nanomaterials, including metal nanoparticles, polymer nanocomposites, and carbon-based structures, has offered unique opportunities to

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enhance the performance and reliability of biosensors. Overall, the chapter strives to deliver an inclusive examination of the advancements including potential future directions in the realm of biocompatible nanomaterials, specifically focusing on their integration into FET-based biosensing devices. It aspires to be an essential resource for researchers, scientists, and practitioners in the field of nanotechnology and biosensing

**Keywords:** Biosensors, and bioelectronics, Field-effect transistor, Nano biosensors, Nanomaterials.

## INTRODUCTION

In the contemporary era, the seamless integration of science and nanotechnology has become a defining feature of our daily existence, profoundly shaping the way we interact with and navigate our physical environment. This transition may be seen in the variety of equipment and gadgets that have become essential in modern lifestyles, including computing devices, smartphones, microwaveable devices, refrigerators, cooling appliances, televisions, and remote controls. These technological wonders, on which we rely for numerous areas of our daily lives, owe their efficiency and functionality to the delicate applications of nanotechnology [1]. At the heart of many of these innovations lie sensors operating at the nanoscale, facilitating precision, automation, and responsiveness. Nanoscience plays a critical part in elevating the performance and interconnection of various technologies, ultimately contributing to the harmonious flow of our daily lives, from the precision of infrared (IR) thermometers to the convenience of remotely operating equipment. The fascination with nanomaterials is driven by the requirement to precisely control substances vital for both the human body and the atmosphere [2]. These materials, which are typically less than 100 nanometers (nm) in at least one dimension (1-D), exhibit exceptional features that have sparked the attention of various applications in medicine, environmental solutions, and different technological advancements. The increased interest reflects a commitment to utilizing nanomaterials to develop personalized solutions to challenging issues [1-15].

Nanomaterials are widely acknowledged for their varied size distributions, ranging from bulk to extremely fine particles, as well as distinguishing characteristics that incorporate a large surface-to-volume ratio (LSVR), quantum mechanics (quantum confinement) effect, enhanced intensity, as well as exceptional sensitivity, which offer an extensive range of advantages over conventional compounds in various domains such as microelectronic devices, healthcare, food processing, agriculture, and pharmaceutical manufacturing. The unique properties of nanomaterials pave opportunities for novel implementations and developments in a variety of sectors, influencing the panorama of current technology and industries. Nanomaterial

synthesis refers to the techniques used to achieve nanomaterials, which are found in nature and are investigated in numerous disciplines comprising physical and chemical science, geology, biology, and microelectronics. These nanomaterials exhibit variations in dimensions, structure, and topology. To acquire its distinctive characteristics, the synthesis process must be carefully regulated, tailoring parameters such as reactant concentration, environmental conditions, and time optimization [3, 4]. A comprehensive knowledge of the components mentioned above is essential for achieving the desired outcomes and may pave the way for the fabrication of multifunctional and revolutionary nanotechnologies. The sustainable synthesis of nanomaterials is the key to uncovering their distinctive characteristics and enabling advancements in a broad spectrum of scientific and technological realms [5-15].

Nanotechnology, a revolutionary discipline at an amalgamation of science and engineering, involves the fabrication, manipulation, and investigation of various techniques, materials, different modes, structural components, and vast applications such as catalysis, fuel cells, quantum-effect lasers, photovoltaic cells, solar transistors, molecular electronic devices, supercapacitors, biosensors, nanoactuators, surface-enhanced Raman spectroscopy, and enhanced energy storage devices. In today's world, nanotechnology has become synonymous with technological advances, particularly in the emergence of biosensors. Researchers are actively exploring the incorporation of cutting-edge nanomaterials, including quantum dots (QDs), nanotubes (NTs), and nanowires (Nws) in the development of biosensor medical diagnostic devices. Nanotechnology has changed biosensor architecture and effectiveness by incorporating several types of nanomaterials and various synthesis modes. The numerous nanomaterials employed in these applications have distinct properties characterized by chemical, physical, mechanical, and surface effects. The quantitative precision enables nanomaterials to unlock an endless number of possibilities, paving opportunities for significant improvements in new devices, notably smart biosensors [16-20].

This chapter provides a meticulous exploration of the current significant advances in biosensor technology, spanning from nanosensors to Field-Effect Transistor (FET) based innovations. The narrative navigates through the details of nanotechnology, highlighting the transformative impact of biosensors operating at the molecular and nanoscale levels. It also delves into the merging of electronics and biology through FET-based technologies [21, 22].

**CHAPTER 5****Advances in the Design and Application of Next-Generation Carbon-Based Field-Effect Transistor Biosensors****D. Anbuselvi<sup>1,\*</sup>, S. Grace Infantiya<sup>1</sup>, N. Suthanthira Vanitha<sup>2</sup>, T. Divya<sup>3</sup> and C. Kathiravan<sup>4</sup>**<sup>1</sup>*Department of Physics, Muthayammal Engineering College, Rasipuram, Namakkal, India*<sup>2</sup>*Department of Electrical and Electronics Engineering, Muthayammal Engineering College, Rasipuram, Namakkal, India*<sup>3</sup>*Department of Computer Science, Velalar College of Engineering Technology, Thindar, India*<sup>4</sup>*Department of Chemistry, Muthayammal Engineering College, Rasipuram, Namakkal, India*

**Abstract:** The proposed book chapter aims to present a comprehensive review of nanomaterial-based biosensors utilizing field-effect transistors (FETs), exploring their diverse applications, advancements, and future potentials. The focus will be on examining the integration of carbon-based nanomaterials into FET-based biosensors and their role in revolutionizing biosensing technologies. Field effect-based biosensors (BioFETs) stand out among other biosensing technologies due to their unique features such as real-time screening, ultrasensitive detection, low cost, and amenability to extreme device miniaturization due to the convenient utilization of nanoscale materials. FET-based sensors operate on the principle that changes in the surrounding environment, such as alterations in temperature, pressure, gas concentration, or biological elements, modulate the electrical characteristics of the transistor. The integration of carbon-based nanomaterials into biosensing applications has emerged as a transformative development, significantly augmenting the efficacy and sensitivity of detection devices, particularly within the domain of field-effect transistor (FET) based technologies. The intent is to provide a holistic view of how these advancements have contributed to improving detection capabilities and to outline potential avenues for further research and applications in the field of biosensing.

**Keywords:** Bio-FETs, Biosensors, Biomolecules, Carbon nanotubes.

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## INTRODUCTION

For one thousand millionths of a meter, the Greek word "nano," which means "dwarf" or "very small," is used ( $10^{-9}$  m). Making a distinction between nanotechnology and nanoscience is crucial. Nanotechnology is the application of knowledge about structures and chemicals at nanoscales, or between 1 and 100 nm, to real-world items like gadgets. Nanoscience is the study of these structures and chemicals [1].

It is significant to remember that a single human hair is 60,000 nm thick, while the radius of the DNA double helix is one nm (Fig. 1) [2]. In the fifth century B.C., during the Greek and Democritus era, the area of nanoscience first emerged. The question of whether matter is continuous and so infinitely divided into smaller parts or if it is made up of tiny, indivisible, and unbreakable components known as atoms was up for debate among scientists.

Nanotechnology is one of the most fascinating emerging technologies of the twenty-first century. It is the ability to monitor, quantify, assemble, regulate, and produce materials at the nanoscale scale in order to put the theory of nanoscience into practice. The National Nanotechnology Initiative (NNI) in the United States defines nanotechnology as "a science, engineering, and technology conducted at the nanoscale (1-100 nm), where unique phenomena enable novel applications in a wide range of fields, from chemistry, physics, and biology, to medicine, engineering, and electronics" [3].

This definition states that two conditions must be met for nanotechnology to exist. First, there is the matter of scale. Utilizing objects by adjusting their proportions at the nanoscale is the main goal of nanotechnology. The second issue is novelty: because of the nanoscale, handling small items in a way that maximizes certain features is necessary for nanotechnology [4-15].

Making a distinction between nanotechnology and nanoscience is crucial. Nanoscience is the combination of physics, materials science, and biology, which deal with the manipulation of materials at the atomic and molecular levels. Nanotechnology is the study, measurement, manipulation, assembly, control, and production of matter at the nanoscale size. There are a few articles available that describe the history of nanoscience and technology, but none that offer an overview of the area's evolution from its beginnings to the present with an emphasis on breakthroughs in the field. Therefore, it is essential to assemble a synopsis of

significant occurrences in this field in order to completely appreciate the progress of nanoscience and technology [16-25].

At the beginning of the twenty-first century, there was an increase in interest in the fields of nanoscience and nanotechnology. National scientific goals in the United States were greatly impacted by Feynman's hypothesis of atomic-level matter manipulation. In a speech at Caltech on January 21, 2000, President Bill Clinton made the case for funding research in nanotechnology. Three years later, George W. Bush signed the 21st Century Nanotechnology Research and Development Act into law. The Act also made nanotechnology research a national priority and established the National Technology Initiative (NNI) [26-35].

## **BRIEF HISTORY OF BIOSENSOR FIELD EFFECT TRANSISTOR (FET)**

### **An Introduction to FET Transistor**

Field-Effect transistors are referred to as FET transistors. An electric field is used by the field-effect transistor (FET) to regulate the current flowing through a semiconductor. FETs have a source, a gate, and a drain on their three terminals. The current flow in FETs is regulated by applying a voltage to the gate, which changes the conductivity between the drain and the source. Julius Edgar submitted the first FET transistor patent application in 1926. Numerous developments have occurred since then. In 1934, Oskar Heil applied for another patent. William Shockley invented the junction gate utilized in field-effect transistors at Bell Laboratories. Over time, FET transistors have seen several more advances [33-35].

### **Working of FET Transistor**

The voltage applied controls the current flowing in a FET transistor, which is a voltage-operated device. Because they operate using a single carrier, they are often referred to as unipolar transistors. All FET shapes and sizes have a high input impedance. The field-effect transistor's terminal applies voltage to control the conductivity in all situations. Furthermore, conductivity is influenced by the carrier charge density. The three main parts of a FET transistor are the source, drain, and gate. The majority of the carriers enter the bar from one of the FET transistor's terminals, which is the source. Most carriers lead the bar via the second terminal, which is called the drain. Two terminals on the Gate are internally linked to one another [35-55].

**CHAPTER 6****Scope and Challenges of Nano-FET for Digital Circuit Design****Jyoti Kandpal<sup>1,\*</sup> and Swagata Devi<sup>2</sup>**

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**Abstract:** Over the previous thirty years, the scaling of complementary metal-oxide-semiconductor (CMOS) technology has stood crucial to the continued advancement of the silicon-based semiconductor industry. However, when technological scaling reaches the nanoscale zone, CMOS devices face several significant challenges, including higher leakage currents, difficulty increasing on-current, massive parameter changes, low yield and reliability, increased manufacturing costs, etc. In order to sustain previous advances, numerous developments in CMOS technologies and device topologies have been developed and put into practice. Simultaneously with these investigations, some innovative nanoelectronic devices, labelled as "Beyond CMOS Devices," are currently intensively investigated and developed as potential replacements or supplements for eventually scaled classic CMOS devices. Despite offering system integration at extremely high densities, these nanoelectronic devices continue to be in their infancy and confront numerous challenges, including high variations and low dependability. The actual implementation of these promising technologies necessitates substantial study at the device and system architectural levels.

**Keywords:** Fin-FET technology, Nanosheet FET (NS-FET), Semiconductor design, Sub-5-nm technology, Transistors.

**INTRODUCTION**

Three broad categories are used by the European Nanoelectronics Initiative Advisory Council (ENIAC) (its prediction shown in Fig. 1) to analyze the silicon-based micro- or nanoelectronics industry:

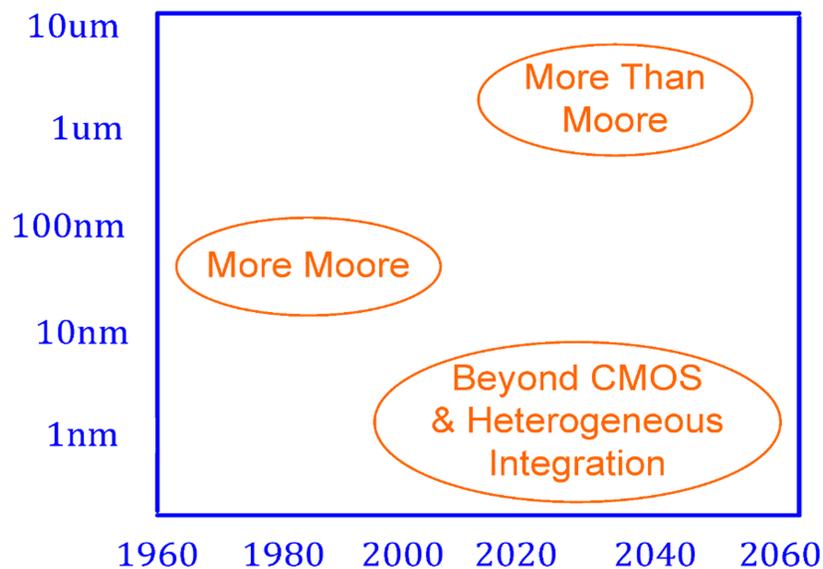
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1. **Advanced CMOS (More Moore):** To continue downsizing transistors, particularly in the improved use of metal gates with suitable work functions, high-k oxides, and high-k oxides as insulators, to ensure an effective throughput while decreasing the leakage via gate stack.

2. **More than Moore:** Fig. (2) shows the concept of more law. Modern CMOS technology has demonstrated itself as inherently constrained. Radiofrequency, analogue circuits, switches with high-voltage actuators, and motion sensors are non-digital functions that call for a combination of technologies customized to a particular need. To overcome these obstacles and implement new features like mechanics, optics, acoustics, ferroelectrics, etc., "more than Moore" is needed.

3. **Beyond CMOS.** New materials, whether inorganic or organic, new operating principles, such as those that replace electrons with magnetic excitation or spin, and new architectural designs, are covered. Examples of alternatives beyond CMOS embrace innovative materials to fabricate interconnects and transistors such as nanowires and carbon nanotubes, switches working with resistive change polymers for memories, the electronic characteristics of organic compounds, memory, and computing architectures to fully utilize the capabilities of these new devices (as shown in Fig. 3).



**Fig. (1).** ENIAC predication for microelectronics future [1].

The designing of electronic systems on a single chip requires optimum exploitation of "system-on-chip" devices, and it will be a vital component of the future of nanoelectronics, integrating "More Moore" as well as "More than Moore" with innovative "heterogeneous integration" technological advances. Another advancement is "system-in-package", which uses different optimized process technologies for combining multiple distinct sub-systems in a single package.

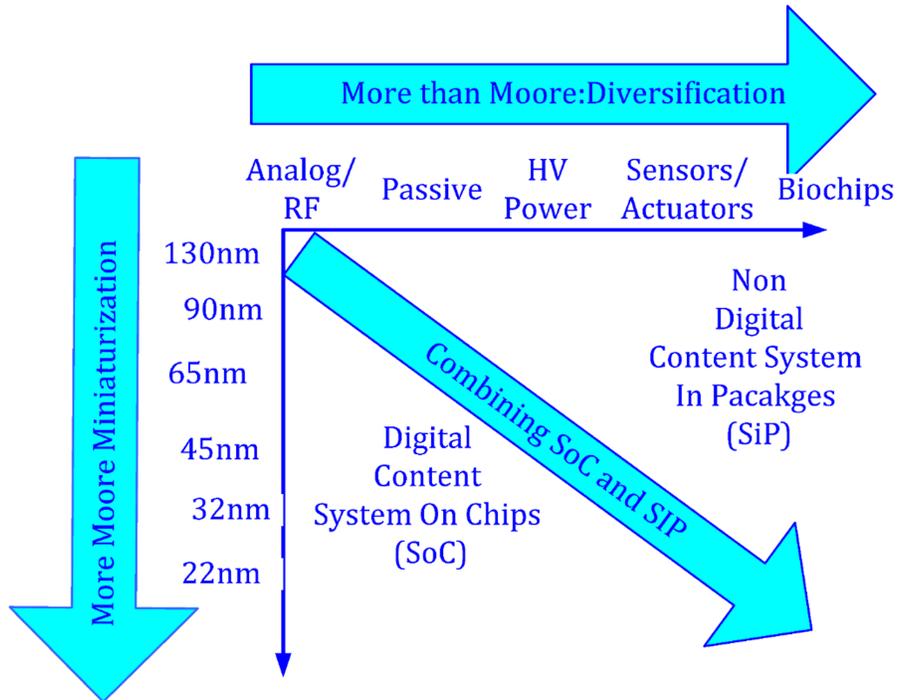


Fig. (2). Moore's law and more [1].

Today's MOSFET is developed at the nanoscale. A tiny chip might contain millions of MOSFETs. When the MOSFET was first designed, it was rather massive and had less functionality than it does now. For decades, engineers have worked to improve MOSFETs' size, power consumption, and other characteristics. As a result, current MOSFET technology has achieved considerable advances. High-performance MOSFETs now have better power handling capabilities and produce less heat. New materials and designs allow quicker switching rates, increasing efficiency in high-frequency circuits. Advanced MOSFETs have reduced on-resistance, allowing for more current flow, and advancements such as silicon carbide (SiC) and gallium nitride (GaN) MOSFETs provide improved performance in high-voltage and high-power applications. Despite advances in current MOSFET

**CHAPTER 7****Analysis and Device Physics of HTFET-based 14T SRAM for Next-Generation Memory Excellence****B.V.V Satyanarayana<sup>1\*</sup>, M. Parvathi<sup>2</sup>, G. Prasanna Kumar<sup>1</sup>, A.K.C Varma<sup>1</sup>, T.S.S Phani<sup>3</sup> and T. Saran Kumar<sup>3</sup>**<sup>1</sup>*Department of ECE, Vishnu Institute of Technology, Bhimavaram, Andhra Pradesh, India*<sup>2</sup>*Department of Electronics and Communication Engineering, BVRIT Hyderabad College of Engineering for Women, Hyderabad, Telangana, India*<sup>3</sup>*Department of ECE, Bonam Venkata Chalamayya Engineering College (A), Odalarevu, Andhra Pradesh, India*

**Abstract:** In this chapter, we address the limitations of device scaling imposed by the subthreshold value restriction of 60mV/decade in the CMOS VLSI design. The focus of current research primarily revolves around effective power methods for cutting-edge electronic devices with additional attributes. Instead of conventional homo-junction MOS devices, our investigation explores the utilization of heterojunctions with SiGe and Ge as these materials have a lower bandgap. By employing a Heterojunction Tunneling Field Effect Transistor (HTFET), we demonstrate a reduction in the subthreshold swing value and achieve low leakage current. We present a revolutionary HTFET design with Gate Oxide Overlap onto Source (GOS) to improve the futuristic features of low-power devices for ultra-low-power memory applications. We implement both n-type and p-type GOS HTFETs, contributing to energy-efficient SRAM cells, by combining low bandgap materials such as SiGe or Ge with high-k dielectrics. The suggested devices show large improvements in Miller capacitance together with a noteworthy decrease in subthreshold swing, high current ratios from ON to OFF, and an increased drive current proportion in the ON state. Expanding the application scope, the proposed device is integrated into a radiation-hardened 14T SRAM cell, showcasing superior performance compared to traditional designs. Memory activities are accelerated, and the chapter concludes with a comparative power and delay analysis of HTFETs-based SRAM cells.

**Keywords:** BTBT, heterojunctions, TFETs, subthreshold swing, SiGe/Ge HTFETs, 14T SRAM.

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## INTRODUCTION

The design and implementation of a low-power SRAM cell specifically suited for ultra-low-power semiconductor memory applications are the focus of this chapter. The main goal is to investigate heterojunction tunnel field-effect transistor (HTFET) topologies at the device level, paying particular attention to important variables including Miller capacitance, ON-state driving current, subthreshold swing, and ON-OFF current ratio. We hope to provide a low-power, low-voltage device that satisfies the requirements of modern semiconductor memory applications by carefully examining these factors [1]. To evaluate the efficacy of the proposed low-power device in practical scenarios, various SRAM cells are essential for circuit-level testing. Consequently, an exploration of different SRAM cell structures suitable for efficient memory devices becomes imperative [2-3]. This chapter elucidates the physical features of the device necessary for optimizing energy-efficient devices and provides insights into various SRAM cell configurations.

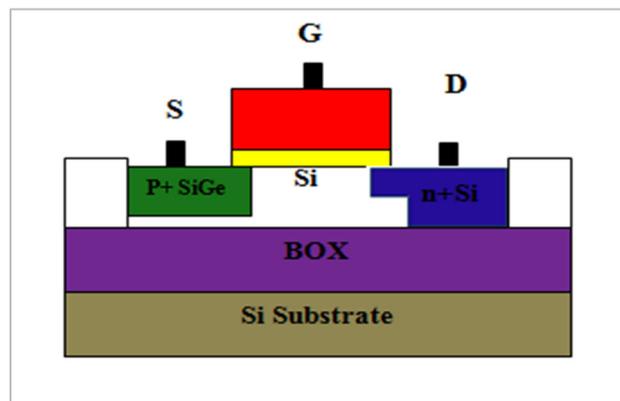
Additionally, this chapter emphasizes the significance of investigating HTFET structures as a pivotal component of the low-power SRAM cell design. The choice of materials, particularly SiGe and Ge, is explored for their low bandgap properties, offering a promising avenue for subthreshold swing reduction below the conventional 60mV/decade limit [4-5]. The incorporation of Gate Oxide Overlap onto the Source (GOS) further enhances device performance, contributing to the achievement of sub-60mV/decade subthreshold swing values and lower leakage currents. Through detailed simulations and validation using TCAD Silvaco tools, the proposed HTFET designs are thoroughly evaluated at the device level, ensuring their suitability for energy-efficient semiconductor memory applications [6-7].

Furthermore, the practical application of the designed low-power SRAM cell is demonstrated through the implementation of a radiation-hardened 14T SRAM cell. Comparative analyses with traditional designs, including 6T, 7T, and 8T memory cells, highlight the superior performance of the proposed device. The read-and-write delays of these memory cells are measured, showcasing accelerated memory activities [8]. Finally, a comprehensive comparison with other state-of-the-art devices, such as conventional HTFET and others is presented. This comprehensive exploration not only advances the understanding of low-power semiconductor memory but also propels the discourse on the practical application of innovative HTFET designs in memory technology [9].

The subsequent sections delve into the comprehensive research findings on Heterojunction Tunneling Field Effect Transistors (HTFETs) and their integration with SRAM cells. Through detailed discussions and analyses, we unveil the intricacies of our research work, shedding light on the promising advancements in the realm of low-power semiconductor memory technologies.

### Analysis of Traditional HTFETs

Heterojunctions emerge as a highly suitable choice for low-leakage memory applications, particularly when integrated into SRAM cells [10]. Substituting homojunctions with heterojunctions in SRAM cells results in a noteworthy reduction in power consumption and delay during read and write operations. Various techniques involving heterojunctions have been proposed by researchers to enhance the performance of these memory cells [11-13]. The structure of traditional HTFET is shown in Fig. (1). The concept of HT Fin FETs, employing a double-gate configuration was introduced in a study [14]. This innovative design optimizes the surface potential, considering the region of overlap. Utilizing the principle of superposition by solving 2D surface potential Poisson's equations, the model is validated with the introduction of  $\text{HfO}_2$  as high-k dielectric. Operating with a fixed output voltage of 0.7V and input voltages ranging from 0V to 0.6V, this approach showcases improved power efficiency.



**Fig. (1).** 2D Structure of traditional HTFET.

The Gate-on-Source-Channel SOI TFETs (GOSC TFET), addressing the reduction in Miller capacitance for enhanced switching speed is proposed in a study [15]. This device, with an input voltage of 0.4V, provides a comprehensive analysis of parameters including output voltage, thickness of oxide, carrier concentration level,

## CHAPTER 8

# Optoelectronic Characteristics of Long Wave Infrared HgCdTe-based Single- and Dual-Junction Detectors

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**Abstract:** Mercury Cadmium Telluride ( $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ ) stands out as the predominant material for developing infrared (IR) detectors. In this chapter, the two-dimensional (2D) p-n (single homojunction and single heterojunction) and p-i-n (dual-heterojunction) architecture models of  $\text{p}^+\text{-Hg}_{0.7783}\text{Cd}_{0.2217}\text{Te}/\text{n--Hg}_{0.7783}\text{Cd}_{0.2217}\text{Te}$ ,  $\text{p}^+\text{-Hg}_{0.69}\text{Cd}_{0.31}\text{Te}/\text{n--Hg}_{0.7783}\text{Cd}_{0.2217}\text{Te}$ , and  $\text{n}^+\text{-Hg}_{0.68}\text{Cd}_{0.32}\text{Te}/\text{n--Hg}_{0.7783}\text{Cd}_{0.2217}\text{Te}/\text{p}^+\text{-Hg}_{0.7783}\text{Cd}_{0.2217}\text{Te}$  are proposed in long-wavelength infrared (LWIR) spectral region. The detectors are designed and analyzed for various optoelectronic characteristic parameters. The outcomes achieved through the Silvaco Atlas TCAD software are compared with those derived from analytical expressions and are found to agree with the analytical results. The proposed detectors are well-suited for their functioning at a wavelength of  $10.6\ \mu\text{m}$  under the condition of liquid nitrogen temperature (77 K). The single homojunction-based detector shows an external quantum efficiency (QE<sub>ext</sub>) of 58.29%, a 3-dB cut-off frequency (f<sub>3-dB</sub>) of 104 GHz with a response time of 3.3 ps, whereas the heterojunction-based detector exhibits a QE<sub>ext</sub> of 67.6%, a f<sub>3-dB</sub> of 265 GHz with a response time of 1.3 ps, and least dark current density. On the other hand, a dual-junction-based detector exhibits a QE<sub>ext</sub> of 84.92%, a f<sub>3-dB</sub> of 1.28 THz with a response time of 0.27 ps, further confirming the suitability of the proposed dual-junction detector for low-noise operations.

**Keywords:** Cut-off frequency, Dark current, Detectivity, HgCdTe, Heterojunction, homojunction, Noise current, Photocurrent, Photodetector, Quantum efficiency, Response time, Responsivity, Spectral response.

## INTRODUCTION

Recently, the field of infrared (IR) sensing technology has witnessed significant progress, driven by the need for high-performance detectors with enhanced sensitivity, broader spectral range, and improved operational efficiency. Among the

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various materials explored for infrared photodetection [1-6], mercury cadmium telluride ( $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ ) has appeared as a promising candidate for enhancing terahertz (THz) and broadband IR detectors, offering improved performance capabilities. This is attributed to its tunable bandgap, low leakage current, relatively high photon absorption coefficient, enhanced stability, low thermal generation rate, moderate dielectric permittivity ensuring small device capacitance, better lattice matching for the growth of high-quality crystals, low thermal expansion coefficient providing device stability, and favorable optoelectronic properties [7-13]. The IR detectors found their major applications in military, optical communications, civilian, thermal and biomedical imaging, remote sensing, missile guidance, fire alarming, gas sensing, satellite remote sensing, motion detection, spectroscopy, surveillance, chemical analysis, telecommunication systems, and night vision. [14-18].

Epitaxial growth of  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  can be achieved as a chemical compound consisting of both HgTe and CdTe. HgTe exhibits a semi-metallic nature owing to its zero energy bandgap and low resistivity, in contrast to CdTe, which is a semiconductor alloy characterized by an energy bandgap of around 1.6 eV. These chemical compounds possess nearly identical lattice constants, enabling the defect-free growth of  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  at any composition. The minimal variation in lattice constant with cadmium (Cd) composition facilitates the formation of high-quality layers and heterostructures. The combination of these materials provides the flexibility to attain energy bandgaps from 0 to 1.6 eV. Since HgTe and CdTe have zinc-blende structures,  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  also has a zinc blende structure for all the Cd compositions [8]. Due to the energy bandgap tunability of  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  via Cd composition ( $x$ ), several high-performance IR detectors based on  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  have been reported. These detectors exhibit various configurations, including p-n [9-18], p-i-n [22, 24], avalanche photodetector [25], barrier detectors [11-13, 26-28], and dual-band IR detectors [10, 29], and have been demonstrated at both cryogenic and room temperatures. The need for cryogenic cooling facilities introduces considerable increases in power consumption, cost, and weight for these IR detectors. The ongoing advancement of  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  technology primarily serves military-related safety or security applications, particularly in the detection of specific conditions or objects. The primary driving force behind considering alternatives to  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  is the technological drawbacks associated with this material. One such drawback is the weak bond between Hg and Te, leading to instability in bulk, surface, and interfaces. Concerns persist regarding yield and uniformity, especially in the long-wavelength IR (LWIR: 8-12  $\mu\text{m}$ ) spectral region [30]. LWIR spectral region encompassing 10.6  $\mu\text{m}$  is well-suited for challenging weather conditions and serves as a strategic atmospheric window. The primary

limitation of  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ -based IR detectors is the elevated dark current restricted by the Auger recombination process and the requirement for working at low temperatures [31, 32]. Therefore it is necessary to create and develop  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$ -based IR detectors that exhibit enhanced performance at or near room temperature. Despite these challenges,  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  continues to be the predominant semiconductor material for IR detectors.

The key challenge in developing any commercially viable detector is integrating it with complementary metal oxide semiconductor (CMOS) technology to deliver advanced detection capabilities. The integration with silicon (Si)-based CMOS technology has garnered extensive interest due to the incorporation of both electronics and optoelectronics on a chip. Si being abundant in nature, is a perfect choice for CMOS technology. It is the primary substrate behind every integrated chip technology. It also facilitates lithography and other fabrication processes in the CMOS technology domain [33-36]. The integration of electronic circuitry follows standard technology, whereas optoelectronic material (such as direct bandgap compound semiconductors) integration with Si (indirect bandgap) is a big challenge due to crystallographic compatibility issues. The real challenge would be to incorporate  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$  as per CMOS process technology due to its incompatibility with Si technology. Despite its Si-based CMOS incompatibility, the lattice-matched  $\text{Hg}_{1-x}\text{Cd}_x\text{Te}/\text{CdZnTe}$  interface is of great interest [23].

The versatility of  $\text{HgCdTe}$  makes it a key material for developing single and dual-junction detectors. Therefore, this chapter aims to provide the two-dimensional (2D) architecture models of  $\text{p}^+-\text{Hg}_{0.7783}\text{Cd}_{0.2217}\text{Te}/\text{n}^--\text{Hg}_{0.7783}\text{Cd}_{0.2217}\text{Te}$  (single homojunction),  $\text{p}^+-\text{Hg}_{0.69}\text{Cd}_{0.31}\text{Te}/\text{n}^--\text{Hg}_{0.7783}\text{Cd}_{0.2217}\text{Te}$  (single heterojunction), and  $\text{n}^+-\text{Hg}_{0.68}\text{Cd}_{0.32}\text{Te}/\text{n}^--\text{Hg}_{0.7783}\text{Cd}_{0.2217}\text{Te}/\text{p}^+-\text{Hg}_{0.7783}\text{Cd}_{0.2217}\text{Te}$  (p-i-n dual-junction) in long wave IR spectral region at liquid cryogenic or liquid nitrogen temperature of 77 K. The detectors are designed and analyzed for various optoelectronic characteristics. The outcomes achieved through the utilization of the Silvaco Atlas TCAD software are compared with those obtained from the analytical model and are found to be in accordance with the analytical expressions. The proposed detectors are well-suited for functioning at a wavelength of 10.6  $\mu\text{m}$ .

## A Review of Nanostructure Field Effect Transistor Devices in Healthcare Applications

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**Abstract:** The evolution of the Nanostructure Field Effect Transistor (Nano FET) has provided significant progress in healthcare applications. Inherent properties such as easy integration, high sensitivity, and better selectivity increased the role of Nano FET devices in wearable electronic devices. Nano FET biosensors have placed great attention in the biomedical field, which performs label-free biomolecule sensing to screen out various diseases. The detection includes cancer biomarkers, cardiovascular diseases, diabetes, HIV/AIDS, DNA and RNA, and viral and bacterial infections. This chapter discusses the overview of diverse applications in healthcare, challenges, and future technologies of NanoFET devices.

**Keywords:** Nano FET devices, biosensors, biomarkers, nanomaterial, clinical applications.

### INTRODUCTION

Currently, sensors based on field-effect transistors have shown superiority because of their remarkable qualities like precision, low operational power requirements, label-free character, economical, and easy surface functionalization. Bio-FET has

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two layers, the bio-recognition layer and the transducer layer, which act as exemplary applicants for Point-Of-Care Testing (POCT) because of its progress in fabrication techniques. Conventionally, Bio-FET sensors are based on novel functional materials such as metal–oxide–semiconductors, organic semiconductors, one-dimensional nanostructured materials (or) silicon nanowires, carbon nanotubes, and two-dimensional nanostructured materials (or) graphene [1-6].

Nanostructured materials are used as channel materials in FET sensors owing to their electrical characteristics, high sensitivity, chemical stability, biocompatibility, and high surface-to-volume ratio. The nanomaterials like nanoparticles, nanowires, and carbon nanotubes have a new approach to biosensing compared to analytical targets. This characteristic facilitates the detection of biomolecules, including proteins, nucleic acids, neurotransmitters, and cancer biomarkers. The scaling of MOSFET offers many field effect transistors on a single chip package facility. One-dimensional nanowire structures are used for the development of a variety of nanoscale semiconductor devices such as FETs, photodetectors, LEDs, biosensors, etc. Biosensors play a significant role in the agriculture and marine industry, surveillance, environmental monitoring, and clinical diagnosis. Biosensors are functional in monitoring health, such as glucose and oxygen sensors, enzyme-based sensors, immunosensors, and pH biosensors [6-12].

A substitute for minimizing short-channel effects in the structure of MOSFET is the nanowire FET (NW-FET). Due to the tunneling effect, drain current and subthreshold swing at extremely small  $V_G$  increase when nanoHUB simulations reduce the channel length from 12 nm to 4 nm. Silicon nanowires (SiNWs) have superior application prospects in the field of biomedical sensing with outstanding electronic properties for improving the sensitivity detection of biosensors [2]. The combination of silicon nanowires and field effect transistors shapes real-time biosensors with great sensitivity and selectivity [13-17].

**Examples:**

1. Zinc Oxide (ZnO), 3, 4 Ethylene Dioxythiophen, Silicon Nanowires (SiNWs), Graphene
2. Indium Gallium (PEDOT), Carbon Nanotubes (CNTs), BlackPhosphorous
3. Zinc Oxide (IGZO)

In recent years, SiNW-FETs have been more focused on the biomedical field for detection. Research groups have been effective in highlighting the primary properties and applications of nanowires to fabricate semiconductor nanowires with controlled diameters. Nanowire detects diseases in the early stage through sensors with high sensitivity. Some classification shown in Fig. (1). The material size decreases in the order of a nanometer. The physical and chemical material properties are determined by the large surface area to volume ratio and quantum size. The main use of nanowires in biomedicine is to identify chemical and biological substances, diagnose illnesses, and aid in drug discovery [5]. Semiconducting nanowires facilitate easier interaction with various electrical signals [18, 19].

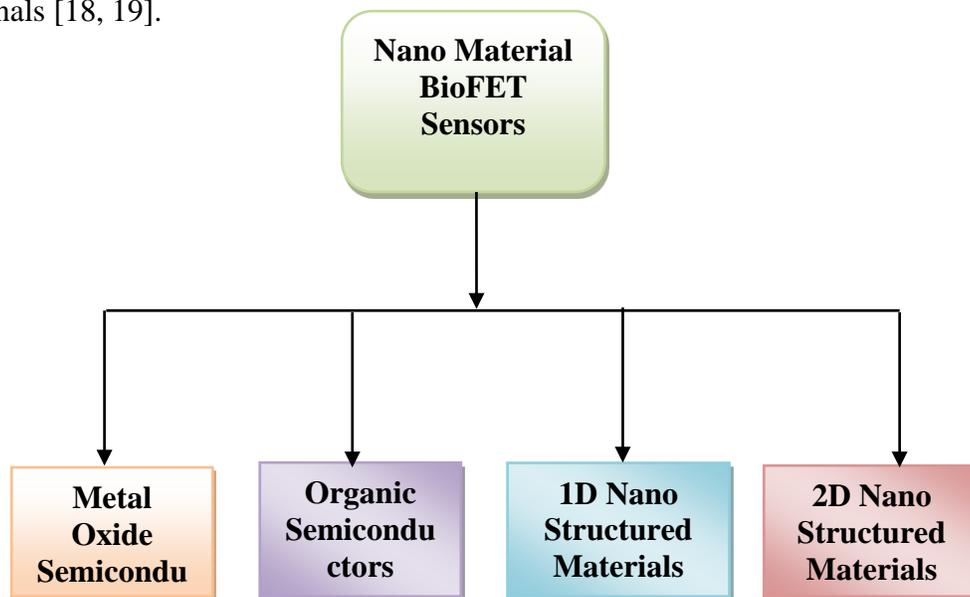


Fig. (1). Classification of BioFET Sensors.

## NANO-FET DEVICES

Nanoscale electrical devices are called nanostructure field effect transistors or nano-FET biosensors. Nano-FET detects and measures the presence and concentration of particular biological molecules [20, 21].

### MOSFET and Nanowire FET

The four terminals of a MOSFET are the source, drain, gate, and body. Conduction does not occur unless a positive voltage is provided between the gate and the source.

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