NANOSCALE FIELD EFFECT TRANSISTORS: EMERGING APPLICATIONS

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PREFACE

The outstanding performance of nanoscale devices in every field of life has grown the researchers' interest in emerging semiconductor nanoscale FET transistors enormously in the last few decades. Nanoscale FET devices promise to be the foundation of the future industrial revolution. This book deals with the modelling, simulation, characterization and fabrication of nanoelectronics semiconductor FET transistors with improved performance in terms of reduced weight and size, improved subthreshold characteristics, improved switching performance, low power consumption, *etc*. The main focus has been given to the essential physics involved in the design of solid-state nanostructures and the performance optimization of these nanoscale devices for emerging real-time applications. The book is dedicated to novel theoretical or experimental aspects of contemporary research relevant to nanoelectronics and semiconductor structures. This book is dedicated to the deliberations on various aspects of nanoscale materials/devices for various applications such as quantum computation, biomedical applications, solar cells, smart lighting, energy generation and storage, sensors, health-care applications, agricultural production, environmental protection, and many more. The book broadly summarizes and discusses the fundamentals of science behind nanotechnology, subthreshold performance, RF/Analog performance, noise and selfheating-related issues, fabrication and characterization techniques, challenges, and applications of advanced nanoscale FET devices. This book gives a general introduction to nanoelectronics and its application to the readers. This book gives a deep insight into evolving possibilities as well as the challenges of nanoscale FETs. This book is well suited for readers of scientific discipline and others working in the nanoscience and technology field. The focus has been given to make the readers well familiar with the world of nanoelectronics and get expertise knowledge in the field of advanced nanoscale FET devices. This book intends to develop interest among readers and researchers towards nanoelectronics and its application in different aspects of life. This book illustrates the basic principles and progress of nanoscience and nanotechnology and also discusses the recent discoveries and milestones in the nanoelectronics field.

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CHAPTER 1

Role of Nanomaterials: In Novel Semiconductor Field Effect Transistors

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Abstract: We are constantly looking to scale down the dimensions of transistors to increase density in the same specific area and at the same time, having powerful functions and increased performance. We have now reached the stage of submicron technology where MOSFETs (metal oxide semiconductor field effect transistors) and FinFETs (fin shaped field effect transistors) cannot be scaled down further. MOSFETs replaced BJTs decades ago, but now transistors seem to have hit their end. While semiconductor giants have a road map to produce 2 nm transistors, scaling down further is next to impossible. Later, FinFETs were considered as their 3-dimensional structure enabled greater density, greater computational power, and lower switching times. But scaling down also means more thermal generation. Thermal effects, high capacitances, and high fabrication costs deemed FinFETs not very suitable for scaling down beyond 7nm. How can we enable transistors to scale down further and follow Moore's law? The next apparent step would be nanotechnology. While it could be a revolution in VLSI it comes with its own cons and challenges. While there is a lot of research going on regarding the same, this chapter will discuss types of nanomaterials based on dimensions like 0D, 1D, 2D, and 3D, and their respective roles in semiconductor FETs and why it is the next sensible step in the semiconductor industry.

Keywords: Carbon nanotubes, Gate all around FETs, Light emitting FETs, Multi-bridge channel FETs, Nanomaterials, Nanowires, Nanosheets, Nanoparticles, Quantum dots, Semiconductor FETs.

INTRODUCTION

Materials with at least one dimension in the nanoscale that is between 1 nanometre (nm) and 100 nanometres are considered nanomaterials. The European

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Commission defines nanomaterials as materials which have at least half of the constituent particles of size 100 nm or less. While nanomaterials share similar composition with their bulk materials, they differ in physical and chemical properties like colour, strength, ductility, conductivity, fluidity, physical state and many more [1].

Nanomaterials can occur naturally, like proteins and lipids in the human body. While some are made incidentally meaning they are produced during combustion, vaporisation, usage, aging, and corrosion of particles. Fullerenes, a class of nanomaterials, are a good example of incidental nanomaterials. The third type of nanomaterials, which is mostly focused upon, is engineered nanomaterials which are engineered and manufactured in particular ways to have specific useful properties.

Nanomaterials have a plethora of uses as they offer many advantages, besides the obvious one of small size, like high strength, high surface-to-volume ratio, increased porosity, ductility, conductivity, and others offering endless possibilities of manipulation of properties and have many applications in military, pharmaceutical, biosensing, cosmetic and other industries [2].

Nanomaterials can be classified based on how many dimensions do not fall in the nanoscale or how many fall in the microscale. For example, 1 dimension in the macroscale means the other 2 dimensions are in the nanoscale, this nanomaterial would be a 1D(1-dimension) nanomaterial.

Below is a Table **1** to simplify the classification:

Table 1. Classification of nanomaterials.

Type of Nanomaterial	Dimensions in Nano/Micro Scale	Examples of Nanomaterial
0D	No dimension in macroscale All dimensions in nanoscale	Nanoparticles Nanoliposomes
1D	1 dimension in macroscale 2 dimensions in nanoscale	Nanowires Nanotubes
2D	2 dimensions in macroscale 1 dimension in nanoscale	Nanosheets, Nanofibers Nanofilms, Nanocoating
3D	3 dimensions in macroscale No dimension in nanoscale	Bulk Materials

The main question is how do nanomaterials fit into the picture of VLSI (very large-scale integration)?

As transistors are scaled down further for smaller size, higher density, lower power consumption, more powerful functions and increased performance, conventional FETs that use Silicon have hit their end. For instance, to make a 2 nm transistor using Silicon, a Silicon atom is 0.2 nm wide so a 2nm transistor is composed of 10 atoms, which make it hard to control the flow of electrons as quantum effects come into play. Sub 10 nm technologies also encounter thermal effects, short channel effects, and tunnelling which make them less effective and less reliable. Hence nanomaterials are the next best alternative. In this chapter, we explore how the three types of nanomaterials can be used in transistors, their principles, applications, and problems.

ROLE OF 2D NANOMATERIALS OR NANOSHEETS IN SEMICONDUCTOR FETS

Nanosheet is a 2D nanomaterial with 1 dimension in the 1-100 nm range. Graphene is the thinnest 2D material made up of a single layer of Carbon atoms with hexagonal lattices is an example of a nanosheet.

As transistor sizes keep scaling down, it gets harder to keep up with Moore's law which states that the number of transistors doubles about every 2 years. After the trend of MOSFETs (metal oxide semiconductor field effect transistors) came FinFETs and then Gate all around (GAA) nanowire FETs. FinFETs used 3 gates and were majorly involved in producing 22 nm, 14 nm, and 7 nm transistors. FinFETs could not be scaled down beyond 7 nm due to problems like leakage current, layout, increasing costs, and decreasing performance issues. GAA nanowire FETs posed parasitic capacitance problems.

About a decade of research later, companies like IBM, Samsung, and Google have arrived at nanosheet FETs to scale down to as low of a size as 2 nm using extreme UV lithography and stacking nanosheets producing transistors with 4 gates.

In 2017, IBM produced a 5 nm chip which is 30 billion transistors dense scaling down from a 7 nm chip that can fit 20 billion transistors. The 5 nm chip is as big as a fingernail with an increase of 40% in performance and 75% in power efficiency than 7 nm technology [3].

Samsung in 2019 introduced 3 nm GAA nanosheet transistors with a 45% reduced area, 50% less power consumption, 35% increase in performance compared to 7 nm technology. Conventional or nanowire-based GAA FETs use a greater number of stacked nanosheets, whereas Samsung’s patented version of GAA-MBCFET (gate all around- multi-bridge channel FET) uses nanosheets enabling greater control over the width of nanosheet and more current per stack [4].

CHAPTER 2

Transition from Conventional FETs to Novel FETs, SOI, Double Gate, Triple Gate, and GAA FETS

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Abstract: Low-power application devices and inexpensive transistors are essential for today's technological world. A 3 nm MOSFET nanoelectronic device has just been created by researchers. Even though a MOSFET shrinks in size and uses less power, SCEs still cause a few problems, leakage current, including Hot electron, Impact Ionization, threshold voltage roll-off, Drain Induced Barrier Lowering (DIBL), and others. One of the best-proposed structures to replace the MOSFET structure is the FIN FET structure, which overcomes the limitations brought on by the CMOS transistor. For low-power applications, the FIN FET structure is ideal. A FINFET structure achieves an average subthreshold swing of 60 mv/decade at room temperature beyond the boundaries of CMOS. This paper examines the performance of the many FINFET architectures that have been proposed, including the double gate, tri-gate, and Gate All Around FET.

Keywords: CNTFET, FET, GAA, IC.

INTRODUCTION

The semiconductor industry has stood for more than 40 years because of the fast growth in product development. The most important trend is the declining cost-per-function, which has significantly increased economic productivity and raised the general quality of life through the widespread use of computers, communications, and other industrial and consumer electronics.

Digital logic, which must offer a technology platform for two different device types—high-performance logic and low-power/high-density logic—takes up a significant amount of the manufacture of semiconductor devices. Speed, density, power, price, capacity, and time to market are important factors to consider while

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choosing a technology platform. The More Moore roadmap provides an enabling vision for further scaling MOSFETs to preserve previous patterns of increased device performance at lower power and cost while still operating at high volume.

The semiconductor industry wants to be able to scale technologies to increase overall performance at lower costs and power. In the past, dimensional Scaling was sufficient to report the best performance benefits, but this is no longer true. Processing modules, tools, material qualities, *etc*., are presenting the difficulties of scalability. Fig. (**1**) shows the short-term (2022-2028) and long-term (2029-2037) challenges to scale the circuit.

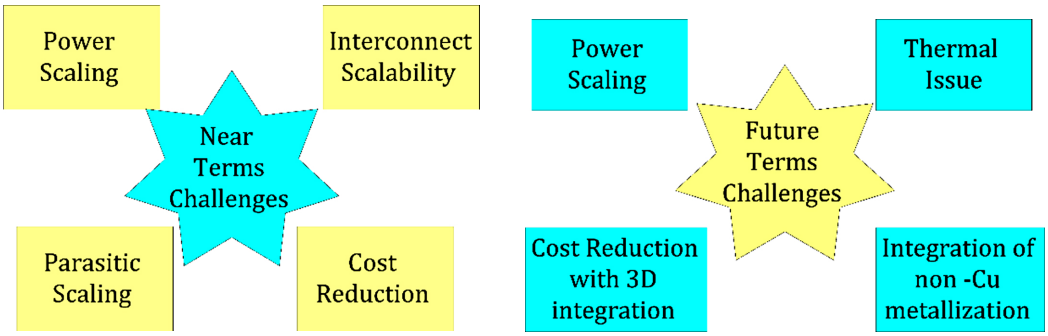

Fig. (1). Challenges to design the chips.

Transistors, the essential building blocks of electronic systems, are widely used. As transistor technology advanced, the transistor's size shrank from the micrometre (m) scale to the nanometer (nm) scale, enabling more transistors in electronic systems. The billions of transistors in the current smartphones, tablets, laptops, supercomputers, and other electronic devices have changed how Scaling minimises the overall device size without compromising performance. There is a limit to growing beyond that; the device does contain unexpected results. Industry and other applications want smaller sizes and portable devices. Gordon Moore made the wise observation that the complication of an integrated circuit (I.C.), as measured by the transistor counts it contains, doubles roughly every 18 months. In the recent era, more than 40 million metal-oxide-semiconductor field effect transistors (MOSFETs) are used at once in the semiconductor industry to produce logic and for better design, mainly focused on transistor density and its interconnection. Fig. (**2**) depicts the following conventional transistor limitations [1 - 3].

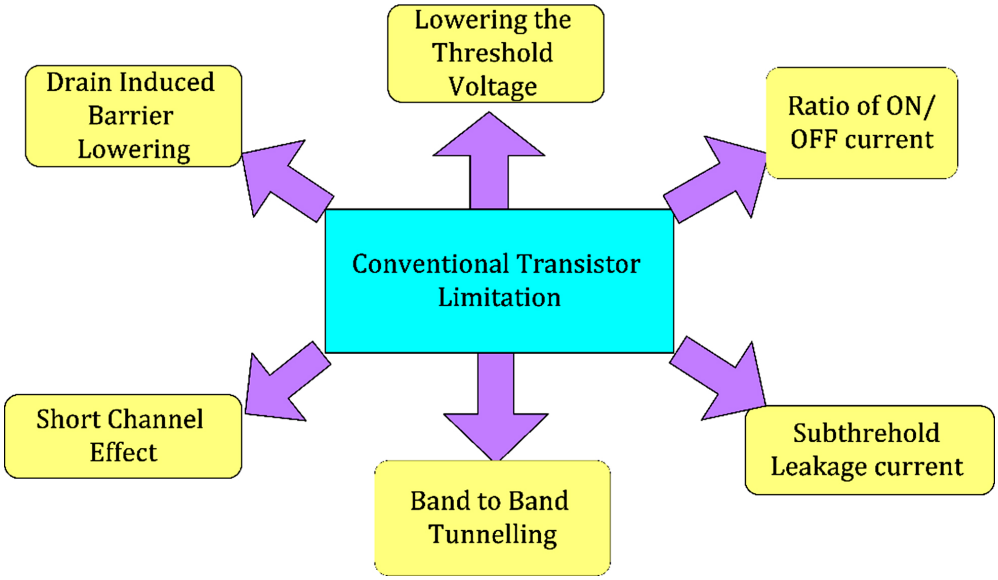

Fig. (2). Limitation of conventional transistor.

Today's semiconductor devices are being pushed beyond their physical boundaries. The system and circuit engineers face challenges with device stability throughout the process. The silicon MOSFET is no longer an ideal alternative. The production yield has also been decreased due to alterations in critical transistor parameters like threshold voltage (Vth), length and width. Scale transistors will require the addition of new device architectures. Innovative devices include modifying bulk silicon to create FinFETs, triage structures, FinFETs, double gate MOSFETs, nanowire transistors and carbon nanotube transistors (CNT).

These FET architectures provide better threshold voltage control, sub-threshold slopes, and short-channel immunity. Additionally, these silicon-different devices may be more scalable and have a larger on-current to off-current ratio.

The semiconductor industry wants to be able to scale technologies to increase overall performance while using less energy and spending less money. Various metrics can be used to assess how well the individual parts and final chip perform, including increased speed, increased density, decreased power consumption, decreased form factor, decreased bill of materials, increased functionality, *etc*. Dimensional Scaling had historically been sufficient to produce the performance above merits; however, this is no longer true. To continue scaling, several

CHAPTER 3

FinFETs and their Applications

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Abstract: Researchers are motivated to develop novel electronic switches with improved low power properties and reduced short channel effects due to the downscaling of conventional MOSFETs (SCE). Using multi-gate FinFET technology could improve control of the gate over the channel charge. We have discussed FinFETs, or multigate transistors, in this chapter. The chapter will include the classification and detailed physics inside the device. The Fabrication section will explain the steps involved in manufacturing the device. The difficulties with FinFET technologies have also been discussed in order to examine the research gap. The performance improvement engineering techniques will give exposure to further improvement techniques in the device. The circuit applications will address the various analog/digital circuits based on FinFET.

Keywords: DFFET, FiNFET, MultiGate transistor, Nanoscale, SOI, SCE.

INTRODUCTION

The advancement of semiconductor technology has led to electronic devices with smaller architectures. Device scaling has the consequence of reducing the gate's controllability over the channel charge and causing disturbed charge flow, which has short channel effects (SCE) [1, 2]. The impact of SCE reduces the device's performance and disqualifies it from scaling down. The semiconductor industry is moving toward multi-gate MOSFETs to boost gate controllability over channel charge. As semiconductor devices become smaller, thermal heating has a greater impact. As the size of electronic devices has gradually lowered to even smaller then the mean free path of materials, there has been a lot of interest in imitating Heat Transfer processes at the micro and nanoscales [3 - 5].

Many novel devices and techniques are discovered and incorporated into the FET based devices to mitigate the short channel effects and make it suitable for the low power and high speed applications. Out of which, tunnel FET is considered a repl-

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acement for the current mechanism of the MOSFET. In conventional MOSFET, the carrier transport is governed with the thermionic emissions but in the tunnel FET, the charge carrier is transferred through the band to band tunneling, therefore, which makes it suitable for the low power applications. Negative Capacitance FET is also emerging as a potential FET based device. In negative capacitance FET, the dielectric material of oxide is replaced by a ferroelectric material or a group of material which should contain at least one ferro-electric material. In Ferroelectric based Fet, there are two states of polarization, one state is switching to another state by the application of the electric field. The negative capacitance FET makes the device suitable for low power microwave applications.

Apart from this, there are several techniques like strained silicon, pocket doping, underlap/overlap and many more to improve the performance of the device.

Nowadays, 2D material based devices are also very popular among device researchers. The 2D materials, in particular, have outstanding electrical, optical, and magnetic capabilities that are drastically different from those of their bulk three-dimensional (3D) counterparts. Additionally, the fast developing synthesis processes enable consistent and precisely controlled deposition of 2D materials in atomically thin layers of excellent quality on a variety of substrates. Such materials' distinctive properties enable a wide range of applications, including flexible electronic devices, harvesting energy, and sensing, merely to name a few. For instance, MoS2's layer-dependent band-gap has been employed to develop ultra-low power transistors, whereas graphene's extremely high mobility combined narrow band gap has been utilized to make ultra-fast interconnects.

In a continuous effort, to improve the drain potential screening from the channel, Planar MOSFETs can be replaced with multi-gate FETs because of the existence of additional gates [6]. The Multi-gate FET refers to the n (where n can be 1,2,3, 4 *etc*.) number of independent gate terminals biased with different potentials formed in three-dimensional devices, as shown in Fig. (**1**).

The two gate FETs are known as Double Gate FETs (DGFETs), and three gate FET refers to tri-gate FETs. The four gate FET is named Quadruple Gate FETs such as Wrapped-Around Gate FET, Gate-All-Around FET, and Surrounding-Gate FET. All of these extra gate FETs are favoured in multi-gate devices because they have lower parasitic capacitances and are more resistant to erratic doping behaviour.

Trigate FETs have a lower fringing capacitance, but the trade-off is a challenging manufacturing process. In this technological age, emerging technologies that consume less power, take up less space and function more swiftly are called

FinFETs [6, 7]. In this chapter, the focus will be on FinFET and its applications which is related to recent trend in the market.

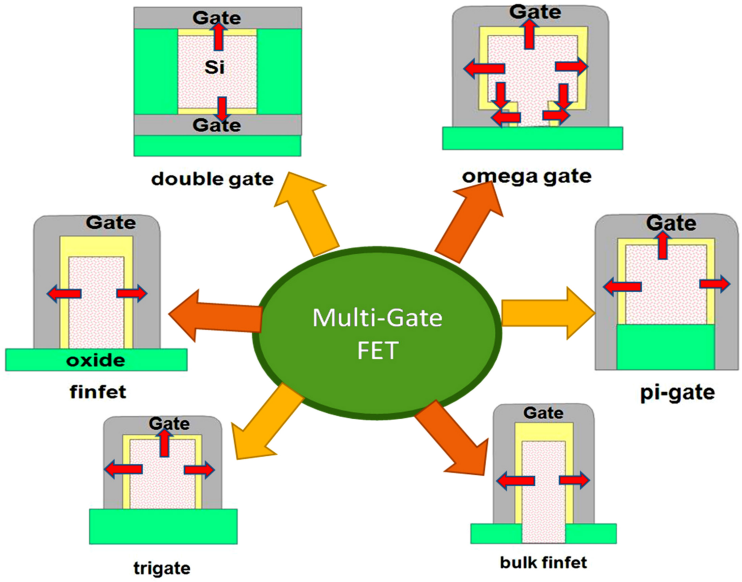

Fig. (1). Different Multi-Gate Structures.

CLASSIFICATION OF THE FinFETs

FinFETs have attracted increasing attention over the past one and half decades because of the degrading short-channel characteristics of conventional MOSFETs [8, 9]. It was the most researched device technology by the leading foundries/industries as well as academia [10, 11]. Therefore, the FinFET technology comes with various architectures as shown in Fig. (**1**) depending upon their usage in device/circuit perspectives, such as double-gate or tri-gate FinFET, symmetric and asymmetric FinFET, tied-gate and independent gate FinFET, and bulk/SOI FinFET. This section will briefly discuss the various classifications and capabilities offered by the FinFET.

FinFETs capture the attention of the market because of their immunity from short channel characteristics, small area requirements, and low power consumption over conventional MOS devices. The FiNFET technology emerges as different types of structures based on their utility from a device/circuit viewpoint. Basically, FinFETs are classified on the basis of 1) Number of Gates 2) Number of terminal 3) Bulk Oxide 4) Symmetricity.

In general, FinFETs can also be categorized as tri-gate and doublegate FinFETs. Both are variants of a FinFET family. With an active third-gate on top of the Si-

CHAPTER 4

Supply Voltage Scaling for Energy Efficient FinFET Logic

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Abstract: A number of ultra-low power applications that don't need high performance can gain power from running at the lowest supply voltage possible. Scaling the supply voltage is a useful technique for cutting the energy needed by digital circuitry. Based on Shannon's channel capacity theorem, the fundamental limit for supply voltage for planar CMOS circuits has been determined to be 36 mV. FinFET devices fit ultra-low voltage applications better than planar devices because of their nearly excellent sub-threshold properties. For the first time, the fundamental supply voltage limit for logic circuits using FinFETs has been defined in this work. It is discovered that this theoretical limit is considerably lower than the limit for planar CMOS devices. On this fundamental limit, the impact of temperature variations and device design characteristics is also investigated. Other logic gates, such as the NAND gate, are included in the analysis. To determine this fundamental limit for a FinFET device, a novel physics-based, semi-empirical current equation valid for supply voltage below 100 mV has been proposed. This is because the operation of a FinFET device in the ultra-low voltage domain differs significantly from that of its planar counterpart. A circuit designer values a current model like this because it makes calculations for back of the envelope calculations simple. The proposed model is then used to study the logic gates functioning in this regime.

Keywords: CMOS Inverter, Device variability, Extensions, FinFETs, Minimum energy, sub-V_{TH} region, Temperature variability, Very low voltage logic design.

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INTRODUCTION

Supply Voltage Scaling

Several applications that need low power consumption while preserving a minimum performance threshold, such as wearable computers, biomedical and IoT systems, portable electronics, *etc*., have spurred a number of notable advancements in deeply scaled V_{DD} (supply voltage) circuit design [1]. A variety of applications that require low power but don't need high performance can gain power from operating at the least possible V_{DD}. Down-scaling V_{DD} is a useful technique for lowering the energy needed by digital circuitry. Limiting the supply voltage to a lower value has proven to be a viable choice for reducing a circuit's overall energy usage. When a circuit switches, the amount of power it uses is given by:

$$P = \alpha C V_{DD}^2 f \quad \textbf{(1)}$$

By decreasing the supply voltage, this dynamic power dissipation can be scaled down in a quadratic manner, albeit at the cost of performance. In some applications, as long as one can maintain the basic functionality, this performance loss is acceptable.

High performance FETs typically combine V_{DD} and threshold voltage (V_{TH}) scaling to maintain a balance between leakage currents and consumed power. However, such scaling is constrained by increasing leakages such gate leakage and sub-threshold current. In planar CMOS-based circuits, the fundamental constraint on the minimum energy dissipated per operation has been well established. In the CMOS digital circuit, a fundamental upper limit for V_{DD} is provided by:

$$V_{min} = 2 \ln 2 V_T \quad \textbf{(2)}$$

[2, 3] for an ideal inverter with a subthreshold factor as 1. This indicates that a supply voltage of 36mV is required for minimum operation at 300K. Using the traditional sub-threshold current equations, the same study has been done for a basic CMOS inverter [4, 5], establishing the limit as 36mV at 300K yet again. This supports the upper bound established using Shannon's channel theorem [3]. The method described in a study [6] serves as the foundation for determining the supply voltage limit for any given technology.

Voltage Scaling in Nanoscale Devices

Well designed Nanoscale devices like FinFETs are more suited for operating in the sub-threshold region than planar MOSFETs because they have superior gate control of the channel than the latter.

They also provide lower DIBL and sub-threshold slope degradation, as well as a greater current drive per unit silicon area [7]. As a result, it is intended to determine the minimal supply voltage requirements for logic circuits based on FinFETs. Due to the considerable modulation of the concentration of charge carriers in the drain extension (DE) with terminal bias, FinFETs operate at ultra-low voltage considerably differently from planar FETs [8, 9]. Many researchers have provided different current models for the sub-threshold operation of FinFETs. In a study [10], a modeling approach utilizing a current source is proposed to effectively address the operation of FinFET devices with independent gate control in the near-threshold region. A current model for the sub-threshold region is derived [11] using the analytical solution of the 3-D Poisson's equation. This work used analytical solutions of Poisson's equation to model FinFETs with doped and undoped channels, accurately calculating subthreshold current and threshold voltage. The study also investigated the variation of subthreshold slope and threshold voltage with device geometry and doping concentration in the channel. In previous studies [12, 13], various analytical two-dimensional current models for the subthreshold region for underlapped DG-FETs were put forth. The graded n-channel underlap FinFET was analyzed using 2-D modeling, investigating the effects of underlap, gate length, and doping concentration of the short channel. These models need a significant amount of computation because they depend on an analytical approach to solving of Poisson's relationship. A current model that provides some basic understanding of the device's physics of operation and is straightforward enough for back-of-the-envelope kind of calculations is preferable to these methods from the viewpoint of a circuit designer. For circuit design, BSIM's [14] Verilog- A based model is a commonly used option. BSIM-CMG is a compact model for bulk and silicon-on-insulator (SOI) complementary metal-oxide-semiconductor (CMOS) technology. It provides a detailed description of the model's features, equations, parameters, and implementation guidelines, along with its applications and limitations. The model is designed to accurately simulate CMOS devices under various operating conditions. The authors [15 - 18] have analyzed the transport in different devices like nanoscale Si MOSFETs, Graphene MOSFETS and Nanoribbons at a mesoscopic level. Nowadays, a number of different Two-dimensional (2D) materials, such as graphene, transition metal dichalcogenides (TMDs), *etc*., are being widely studied for their unique electronic and optical properties. These materials have the potential to revolutionize electronic device technology due to

CHAPTER 5

Graphene FET for Microwave and Terahertz Applications

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Abstract: A graphene based FET can be used for a variety of applications. It can be utilized in the fascinating field of nano-scale device electronics or microwave and terahertz based guided wave components. In this chapter, a review of graphene field effect transistors has been presented in RF and bio-sensor circuits. It begins with an overview of the superior properties of graphene in graphene FETs, moving further to the characterization and fabrication challenges, and thereafter, their application in bioanalytical sensing and high frequency devices has been investigated. Graphene material has potential advantages in the form of low losses and power dissipation due to its high thermal, electrical conductivities and mobilities. It leads to better performance and efficiency relative to its silicon counterparts in various applications. It has some design and fabrication challenges owing to its high surface density and single atomic thickness. It also shows limitations in terms of bandgap variation, high fabrication costs and current saturation features.

Keywords: Biosensing, Detectors, Graphene, High frequency devices, Terahertz.

NATURE OF WORK

The nanoscale devices have revolutionized the world of semiconductor device technology [1]. New materials have been explored, which have led to the development of carbon nanotube (CNT) based FETs and FinFETs [2]. FinFETs are promising candidates for future nanoscale devices in terms of performance and features. CNT based FETs have potential advantages as compared to conventional silicon technology. The strong covalent bonds, along with high mobilities, lead to high mechanical and thermal stabilities.

Strong in-plane covalent and feeble interlayer van der Waals bonds characterize layered crystals that are two dimensional (2D) materials. These materials contain

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a variety of unusual chemical, mechanical, optical, and electrical properties that allow for the development of new technological products and systems as well as a platform for the study of fundamental physical processes. High-performance radio-frequency (RF) devices and plasmonic photodetectors utilize monolayer molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2). For instance, the MoS2-based FET was created for the first time in 2011 and later included in the first generation of chips. It has recently emerged as a possible candidate material for high-performance integrated circuits, lowering the contact resistance of single-layer two-dimensional semiconductor MoS2 to 42 Ω·μm by increasing the hybridization of semi-metal and two-dimensional semiconductor interfaces' orbitals. Thus, the researchers have been able to surpass the contact resistance of silicon-based transistors connected by chemical bonds and get close to the theoretical quantum limit. With this accomplishment, a major barrier to two-dimensional semiconductor applications in high-performance integrated circuits is removed. The world's fastest and least energy-intensive two-dimensional semiconductor was recently created by a research team at Peking University, who created 10 nanometer ultra-short channel ballistic two-dimensional indium selenide transistors. This is the first time that practical two-dimensional transistor performance has surpassed that of silicon-based Fin transistors at Intel's commercial 10 nanometer node. A high-performance two-dimensional fin-type field effect transistor has also been developed along with the first epitaxial growth of a two-dimensional semiconductor fin/high-κ gate oxide heterojunction array ever reported in the world [1, 2].

A graphene based FET can be used for a variety of applications. It can be utilized in the fascinating field of nano-scale device electronics or microwave and terahertz based guided wave components. This chapter provides an overview of graphene field effect transistors in RF and biosensor circuits. It begins with an overview of the superior properties of graphene in graphene FETs, moving further to the characterization and fabrication challenges, and thereafter, their application in bioanalytical sensing and high frequency devices has been investigated. Graphene material has potential advantages in the form of low losses and power dissipation due to its high thermal, electrical conductivities and mobilities [1]. It leads to better performance and efficiency relative to its silicon counterparts in various applications. It has some design and fabrication challenges owing to its high surface density and single atomic thickness. It also shows limitations in terms of bandgap variation, high fabrication costs and current saturation features [3].

INTRODUCTION

MOSFETs have been investigated as a major component of electrical device circuits. The thermal behavior in these transistors has been studied using the Robin boundary condition and temperature jump boundary condition [4]. Various mathematical models have also been developed for observing heat conduction in these nano-transistors [5]. The use of graphene material in MOSFETs has enhanced their properties to be used for utilization in nanoscale devices [6]. The thermal stability improves in graphene FETs [7].

Graphene, the wonder material, has become the talk-of-the-town among researchers, scientists and investigators. Along with Konstantin Novoselov, Andre Geim's Nobel Prize-winning discovery in 2010 in Physics is truly remarkable [8]. It evolved the theoretical and experimental investigations with materials for utilization in active and passive circuits [9]. The material has impeccable properties influencing microwave and high frequency regions of several devices like transistors, filters, antennae, *etc*. Its physical properties in these regions are excellent and unobserved till now in existing materials. The properties of graphene will now be discussed in the following section.

PROPERTIES OF GRAPHENE

The single layer allotrope of carbon has several exciting properties, making it stand high for explorations among a large community of researchers [10]. It is only one atomic layer of crystalline atoms of carbon with a hexagonal grid configuration, as shown in Fig. (**1**). If the atomic layers of graphite are removed, graphene is obtained. These layers are connected loosely by means of forces of Van der Waals', that were isolated physically for the first time in the year 2004. Apart from being crystalline in nature, it has high thermal conductivity. It is flexible as well as strong, even at nanoscale thicknesses. Even being transparent, it absorbs large amounts of light. It can be used in the detection of chemicals, but it is stable and non-reactive. It forms the channel for carriers, allowing a high surge of electronic charges to pass through it, owing to its high electron mobilities, even higher as compared to conventional materials like silicon, gallium arsenide, gallium phosphide, *etc*. Thus, graphene possesses high mechanical strength at nanoscale thicknesses, crystalline nature with high electrical and thermal conductivity, good absorbent with optical transparency, stable and impermeable in nature [11].

CHAPTER 6

Analysis of Negative to Positive Differential Conductance Transition in NCFET and Guidelines for Analog Circuit Designing

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Abstract: In this chapter, we explained a detailed physical insight of Negative Differential Resistance (NDR) to Positive Differential Resistance (PDR) transition in a ferroelectric-based negative capacitance (NC) FET and its dependence on the device terminal voltages. Using extensive well-calibrated TCAD simulations, we have investigated this phenomenon on FDSOI NCFET. The NDR to PDR transition occurs due to the Ferroelectric (FE) layer capacitance changes from a negative to a positive state during channel pinch-off. This, in turn, results in a valley point in the output characteristic (IDS-VDS) at which the output resistance is infinite. We also found that we could alter the valley point location by modulating the vertical Electric field through the FE layer in the channel pinch-off region using body bias (V_{BB}). The interface oxide charges also impacted the NDR to PDR transition, and a positive interface charge resulted in a faster NDR to PDR transition. Further, we have utilized the modulation in NDR to PDR transition due to VBack for designing a current mirror. Results show that the output current (I_{OUT}) variation due to V_{DS}, reduces from ~8% to ~2% with VBack. We have also designed a single-stage common source (CS) amplifier and provided design guidelines to achieve a higher gain in the NDR region. The results obtained using a small-signal model of the FDSOI-NCFET demonstrate that ~25% higher gain can be achieved with the discussed design guidelines in the NDR region compared to the transition region of I_{DS}-V_{DS}. We have also explored the device scaling effect on the amplifier gain and found that ~2.23x gain can be increased with a smaller channel length and higher device width.

Keywords: Fully depleted silicon-on-insulator, Ferroelectric polarization, Negative capacitance, Negative differential resistance, Positive differential resistance.

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INTRODUCTION

The scaling of the transistor at one side has tremendously reduced the power requirement and has increased the ON current and the transistor density. This could be possible in all these years due to Moore's prediction about aggressive scaling. On the other side, the scaled transistor loses the vertical field control due to the short channel lateral field effects. Therefore, the transistor becomes leaky and subthreshold characteristics deteriorate. These short channel effects affect the Figure of merits (FOMs) such as OFF current (I_{OFF}) and I_{ON}/I_{OFF}, and these FOMs are required to design the digital and analog circuits [1, 5]. To overcome those short channel effects (SCEs), some engineered techniques such as strained-silicon, metal gate, source and drain regions have been introduced. The researchers have also looked for the geometrical changes in the devices [6, 7]. In the non-planar and planar short channel devices, *e.g*., FinFET, gate all around, and Fully-Depleted-Silicon-On-Insulator (FDSOI), Tunnel FETs have been investigated. The Tunnel FETs provide the steep subthreshold swing due to the tunnelling mechanism, but it suffers from the low ON drive current, and thus, it is not suitable for high-performance applications [8, 10]. Therefore, till now, the mainstream fabrication industries have focused on FinFETs and FDSOI-based technologies. The non-planar FinFET gate-all-around technology shows excellent electrostatic gate control due to the availability of multiple gates. But it suffers from higher parasitic capacitances [11, 12]. Conversely, FDSOI offers better electrostatic control than the MOSFET [13, 15]. It is a planar structure with a comparable subthreshold swing to the FinFET despite being the single gate control device [16, 17]. But both the advanced planar and non-planar technologies are unable to overcome the Boltzmann tyranny of 60 mV/decade, and sub-10nm device scaling with a reduction in the power supply is challenging with the existing technologies. In the series, the concept of negative capacitance is a powerful tool to break the Boltzmann limit. NCFETs are devices in which the oxide layer of higher permittivity is replaced with the ferroelectric oxide layer [18]. The ferroelectric oxide layer shows polarization stable states in the polarization-electric field (P-E) loop, and the negative capacitance region is the unstable region in between the two stable polarization states. Thus, the unstable region is not visible in the isolated Metal-Ferro-Metal capacitor, but with the positive capacitance in series, it can be stabilized with the concept that the total capacitance of the system must be positive. As mentioned, the ferroelectric layer offers a negative capacitance that can be stabilized; therefore, in the NCFET, the surface potential gets amplified due to the internal voltage amplification by the ferroelectric negative capacitance.

NCFET ARCHITECTURES

NCFET can be designed with two different device architectures.

a. Metal-Ferro-Metal-Insulator-Semiconductor (MFMIS) FET.
b. Metal-Ferro-Insulator-Semiconductor (MFIS) FET.

Metal-Ferro-Metal-Insulator-Semiconductor (MFMIS) FET

In MFMIS FET, the Metal-Ferro-Metal is bonded to the underlying transistor, as shown in Fig. (**1**), and thus, the internal metal gate (IMG) potential gets the amplified potential [19]. The Potential at IMG decides the surface potential, and therefore, due to amplified IMG, the surface potential gets amplified even without increasing the applied gate potential.

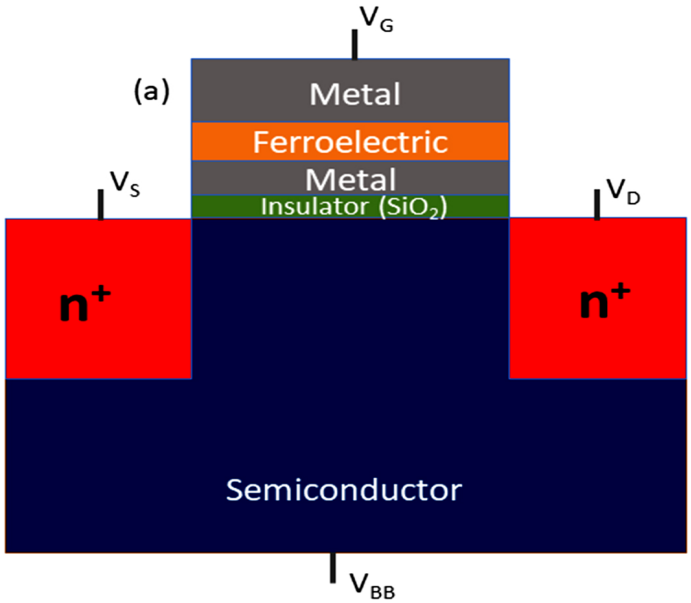

Fig. (1). Pictorial Representation of MFMIS FET. The symbols V_{BB}, V_G, V_S, and V_D show the substrate, gate, source, and drain terminal voltages, respectively [19].

Metal-Ferro-Insulator-Semiconductor (MFIS) FET

In MFIS FET, the internal metal gate is not present. The high-k oxide layer is directly replaced with the ferroelectric oxide layer, as shown in Fig. (**2**). In MFIS NCFET, as the V_{GS} is applied, the potential drop inside the ferroelectric layer is opposite to the drop inside the interfacial oxide layer due to the negative capacitance property of the ferroelectric layer. Therefore, in this way, there is a net amplification in the potential received by the channel. In the MFMIS NCFET,

CHAPTER 7

CMOS Compatible Single-Gate Single Electron Transistor (SG-SET) Based Hybrid SETMOS Logic

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Abstract: The continuous development of CMOS technology today beyond many obstacles has been witnessed by all of us. After three decades of aggressive scaling to ever-smaller dimensions, today, MOSFET gate lengths can be less than 22 nm. There are many challenges and limitations at the device level. Short channel effects, such as drain induced barrier lowering, Vth roll-off, gate induced drain leakage, static leakage, punch through, and contact resistance, are among the major blockades for sub-22 nm technology. Many physicists have explored this extremely small dimension device and the effects of charge and energy quantization, and that emerged the concept of single electron conduction. Single-electron devices were being seen as one of the finest beyond-CMOS nanodevices reported by many researchers and ITRS. These devices were facing many roadblocks due to their ultra-small dimensions, fabrication viabilities, room temperature operation, CMOS compatible processes, and lack of simulation methodology. Since the last decade, the evolution of advanced e-beam lithography, Chemical-Mechanical polishing and deposition techniques has gained many researchers' attention, and the trend to explore these devices is going continuously in an upward direction. Though it is difficult to replace CMOS technology completely, the hybridization of these devices with CMOS is one of the major interests shown by many research works.

Keywords: Beyond CMOS nanodevices, Coulomb Blockade (CB), Hybrid SETMOS logic, Quantum-Mechanical Tunneling (QMT), Single-Electro--Transistor (SET), Ultra-low-power logic circuits.

INTRODUCTION

Besides CMOS, nanodevices are investigated tremendously for ultra-low-power applications for many years. By virtue of scaling in CMOS, degradation arises in the performance of the circuits.

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This ultimately opens the door for novel nano devices either to succeed in CMOS or to hybridize with existing technology. A huge study has been conducted for 2D devices, spin-based devices, vertical FETs, SOI FETs and Fin-based devices for two decades [1]. The CMOS fabrication compatibility, room temperature operation, low leakage current, high-speed operation, circuit design using new physical principles, and large-scale manufacturing are some of the key challenges for novel nano-devices [1]. In the era of nanoelectronics, Single Electron Transistors (SETs) can be the most promising nanodevice for logic as well as memory applications [1]. Multiple researches have been conducted to ensure SET operation starting from 1985-87 by Likharev [2]. The work done by Lee [3], Dubuc [4, 5], Sun [6] and Joshi [7] demonstrated SET fabrication using CMOS compatible processes. Uchida [8] and Mahapatra [9, 10] showed the pioneer work to model SET for circuit design along with CMOS compatibility. Recent works have been conducted in the direction of Hybrid SETMOS design and its optimization [11 - 15].

SET is working on quantum physics principles: Coulomb Blockade (CB) and Quantum Mechanical Tunneling (QMT), portraying its OFF and ON states, respectively. As shown in Fig. (**1a**), unlike MOSFET, SET consists of a conductive island (shown as QD), surrounded by two tunnel barriers on the source and drain sides.

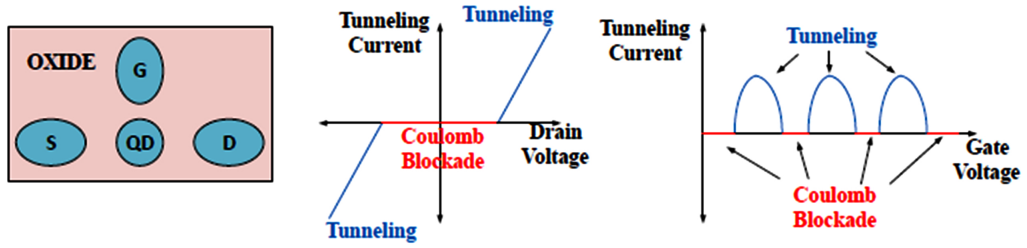

Fig. (1). SET representation, Output characteristics and Transfer characteristics.

These tunnel barriers provide sufficient barrier height to prevent the conventional electron flow, which is also known as the Coulomb Blockade. These barriers are ultra-thin (in the nm range) and make sure weak coupling of the source and drain with the conductive island. So, an electron from a source with sufficient energy can enter the island after overcoming the Coulomb Blockade energy level by the process of tunneling. Simultaneously, an electron tunnel from the island to the drain causes the flow of the electron current. The output characteristics Fig. (**1b**) show the same phenomenon in which the CB can be overcome after drain bias called CB voltage. After CB voltage, the tunneling state can be observed. The

transfer characteristics Fig. (**1c**) illustrate Coulomb oscillations of drain current. It is observed by varying gate voltage for fixed drain current, and due to this, CB and QMT occurred periodically.

Thus, to ensure the charge transfer, Coulomb Energy can be supplied by an external voltage source to the island [16 - 18],

$$E_C = \frac{e^2}{2C_\Sigma} \quad \textbf{(1)}$$

where, C_Σ is the total capacitance of the conductive island given by ($2C_J + C_G$). C_J and C_G are tunnel junction and gate capacitance. Correspondingly, Coulomb Blockade Voltage is given by:

$$V_{CB} = \frac{e}{2C_\Sigma} \quad \textbf{(2)}$$

This total capacitance is mainly controlled by the device dimensions and material. With the reduction in C_Σ, E_C increases, creating the junction opaquer. The tunnel barriers offer tunnel resistance, and this must be greater than the essential quantum resistance ($R_T \gg h/q^2$), *i.e.*, approximately $\gg$ 25.8 KΩ [16 - 18]. It confirms the localization of electron states to the conductive island during the Coulomb Blockade. R_T also limits the driving capability of the SET. The maximum operating frequency is proportional to $1/(R_TC)$ [11]. Conflict of device speed and power dissipation can consequently be tackled by excellent setting of these two device parameters. This necessitates proper materials choice and fabrication of capacitors of the order of attofarads. The CB and QMT have been observed at low temperatures due to their ultra-small (in a few nm) dimensions [2, 9, 19]. However, research on its room temperature operation is succeeded by many due to advancements in lithography, chemical mechanical polishing (CMP), ultra-thin dielectric growth and deposition techniques [4 - 6, 20]. The low-current drive and low supply voltage were issues for CMOS compatibility [17, 19 - 21]. However, it was attained and overcome [4, 22, 23].

Research to exhibit room temperature behavior analogous to a conventional MOSFET and its demonstration for application in logic and memory circuits is still in infancy. The proper design methodology from the device level engineering to circuit design is a need. The advantage of silicon processing further enhances the SET to hybridize with existing CMOS for ultra-low power dissipation without losing functionality [8, 9, 24, 25]. There are many techniques for hybridization of

CHAPTER 8

Extensive Investigation on Even-Transistor-Configuration CMOS-based SRAM

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Abstract: Designing electronic devices with higher efficiency while using reduced power is a problem in the field of electronics. Digital technology utilization is increasing due to its higher speeds, lower power requirements, and stability. Accessing data requires a lot of time, so a circuit is created that will be close to the CPU to provide the information that is required. Cache memory is a type of SRAM-based faster storing device. To enhance the performance of the SRAM cell, Read Delay (RD), Write Delay (WD), read stability, write stability and power dissipation of the intended circuit should all be carefully considered while designing an efficient SRAM cell. Delay, power dissipation, and circuit stability all trade-off with one other. In this chapter, we will look at delays, average power dissipation (APD), and stability using a variety of cell ratios, pull-up ratios, and supply voltages, and compare how each of these metrics has improved. As miniaturization of post CMOS technology, technology nodes are getting smaller. Because of this, researchers have examined different typologies, ranging from 6T SRAM to 12T SRAM (even-number transistor cell) analysis. Better delays and an improved static noise margin are obtained by increasing the number of transistors per cell, although power dissipation increases as a result. This chapter covers the overall analysis for SRAM cells with 6T, 8T, 10T, and 12T transistors that vary in CR and PR as well as voltage. The circuits are created for the overall study using a 180nm technology file in the Cadence Virtuoso tool.

Keywords: Average power dissipation, Read delay, Read static noise margin, Write delay, Write static noise margin.

INTRODUCTION

Electronic devices throw a challenge to make devices with greater performance with low power. Immense usage of electronic products is gaining attention for faster speed, less power consumption, and stability [1, 2]. For faster speed of operations, accessing data takes a lot of time, so a circuit is made which will be

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close to the processor to supply the required data [3]. A faster memory device is named cache memory, which is made up of SRAM [4]. It is static in nature, no refreshing mechanism is needed. SRAM comes under volatile memory, which means holding data till supply is high. SRAMS are used in devices that need processors like mobiles, laptops, computers, *etc* [5]. DRAM also stores data, but it is refreshed periodically to retain the data, which needs a refreshing circuit [6]. Due to this reason, DRAM works slower. SRAM became a better choice for speed of operation and power dissipation.

The conventional configuration of SRAM is made up of CMOS-based six transistor cells; this became the most commercially used topology for cache memory design [7, 8]. We require a memory that has a quick response time since the pace at which devices and high-speed clocks operate is constantly increasing [9, 10]. There is hardly any convergence between the speeds of the processor and the memory. In order to speed up memory, researchers are experimenting with various topologies, such as increasing the total number of transistors and proposing novel SRAM cell configurations. In this chapter, we investigated even number transistor configurations like 6T, 8T, 10T, and 12T topologies. As in achieving fastness, we sacrifice power because as we increase the number of transistors, power dissipation and leakages also rise. So, we need to make trade-offs with speed and power dissipation [11, 12]. Stability is also one of the major parameters as due to a decrease in technology nodes, we reduce supply voltages from that stability also decreases. To improve stability, we use Cell Ratio and Pull up ratio and varying them improves the stability of the circuit. Achieving this stability is due to an increase in the cell ratio and pull-up ratio capacitance of the device increase which makes the device slower and dissipates more energy [13, 14]. So, we need to engineer a circuit that satisfies a good delay, low power, and stable circuit.

Several SRAM cell topologies are determined by the number of transistors employed during the fabrication of the memory cell. We access 6T-12T SRAM combinations. The typical 6-transistor (6T) SRAM cell is widely used because of its straightforward design. The latency and power efficiency of the even transistor based SRAM cell are respectable. In addition, the strong noise immunity and reduced leakage current in the cell contribute to its low static power dissipation. The conventional 6T SRAM design and other even transistor configurations can be examined to be improved upon in order to significantly lessen power consumption [12 - 14].

VARIOUS TOPOLOGIES OF SRAM AND ITS OPERATION

6T SRAM and its Operation

The 6T SRAM has a pair of inverters that are connected back to back, as shown in Fig. (**1**), which resembles positive feedback that holds bit values ”0” or ”1”. Two-pass transistors are used to enable the path for reading and writing required data to the SRAM cell. Before read or write operations, we pre-charge the circuit to maximum voltage with the help of a separate pre-charge circuit [15, 16]. We will write data into the SRAM with the help of a circuit named write driver. We extract the data present in the cell is based on the difference in voltage levels in bit lines BL and, BLB which is detected by the sense amplifier circuit.

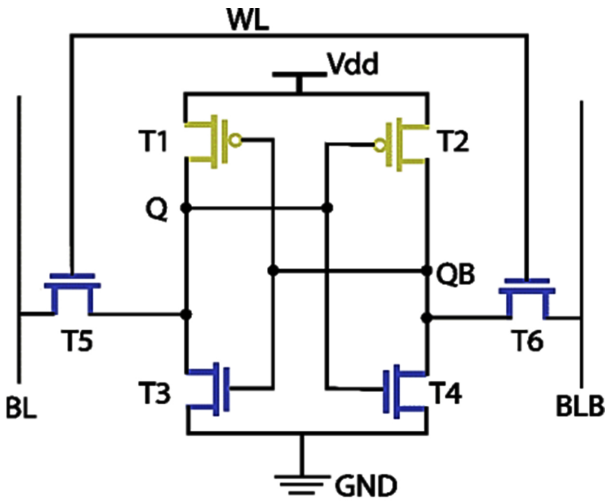

Fig. (1). Interpretive illustration of the 6T-SRAM cell.

Hold Mode

In this state, the pair of access transistors is turned off by whatever data is previously present, which will be maintained in a positive feedback-connected inverter cell.

Read Mode

For reading the stored data, we must precharge bit lines to a high value before reading and enable a high value by a word line (WL). From Q and QB, one node will be lower, which makes a smooth path to discharge from any one of the BL or BLB bit lines. For this, a circuit named a sense amplifier is used to find the difference in signal at both nodes, and it will be given as output.

CHAPTER 9

A Comparative Analysis and Ideas to Reduce Various Leakage Power in Modern VLSI

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Abstract: In today's high-performance chips, comparative analysis and ideas for reducing power consumption have become the dominant factor in overall power consumption. This should reduce the power consumption of high-density chips, which is so great that many new techniques have been developed in the proposal to design low-power circuits and systems. Ultra-thin gate oxides, very low threshold voltages, and short channels are hallmarks of nanoscale chips. Therefore, the most difficult problem that arises in VLSI circuits and systems is power dissipation. This paper provides an overview of sources of leakage currents in sub-micrometer CMOS gates and techniques, limitations, analysis and ideas to reduce leakage currents [1]; an overview of current circuit-level leakage currents [2] for various techniques; also discusses an example of a 1-bit adiabatic ECRL adder which compares the power and delay. This is one way of leakage minimization technique which is caused by switching action. This simulation work is done in cadence tool using FINFET technology which is a very fast-growing technology as compared to CMOS technology [3].

Keywords: Leakage power, Ultra-thin gate oxide, Very low threshold voltage and short channel.

INTRODUCTION

In recent years, there has been a push to make more long-lasting, faster-processing, and less space- and power-hungry gadgets, laptops, handsets, *etc*. This describes the reasoning and methods used to lessen a CMOS circuit's power consumption [2]. Each CMOS module receives the same amount of power regardless of how many there are. This is the maximum allowable current drawn by the subsystem. A well-balanced design can only be achieved by adhering to a

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number of constraints, one of which is the restriction on power consumption distribution.

Power can be lost in a number of different ways, but they can all be reduced. In order to create circuits with minimal power consumption, CMOS is used. Since leakage is proportional to the square of the diffusion area, using compact devices is preferable. The power consumption of the components is an important factor to consider during system design. By lowering the supply voltage, the switching capacitance and the logic clock frequencies, dynamic power consumption can be reduced.

Modern electronic systems have made energy efficiency a basic component due to the prevalence of portable electronics, the need for consistent quality and performance, the desire to extend battery life, the need to reduce total costs, and similar factors. Progress in scaling has led to lower limit and supply voltages, which has led to an increase in leakages in MOS semiconductors. Multiple studies have found that absolute power utilisation in nanoscale technology accounts for forty percent of the ultimate spillage power usage [2]. To address the issue of power dispersal, numerous professionals have proposed a wide range of solutions, some at the device level and others at the design level. Despite this, there is no generally agreed-upon method of avoiding compromises in resource allocation, timeliness, or physical location.

As a result, new product developers have a responsibility to select methods that are well-suited to the task at hand. Power consumption in VLSI circuits can be tightly regulated by adjusting the supply voltage. When the supply voltage is decreased without correspondingly increasing the edge voltage, the device's display is diminished [3]. Edge voltage is reduced, and supply voltages are increased relatively to keep the show going. The spilled current increases by a factor due to the drop in edge voltage [4]. Power efficiency enhancements are becoming increasingly important, and the reasons for doing so can vary widely between applications. We have looked into the many methods available for reducing leakage power in VLSI circuits.

BRIEF ON LEAKAGE CURRENT COMPONENT

An integrated circuit consists of different blocks; each block works with different frequencies, but the high frequencies should have a limit for power consumption in computer systems or any other gadgets so power used by each device should be minimum. Power calculations are used to determine power distribution sizing, current requirements, thermal efficiency, and device selection criteria. Power calculations can also be used to determine the most reliable operating frequency.

A CMOS circuit's power consumption is determined by two components:

- Static power consumption
- Dynamic power consumption

CMOS devices have very less static power consumption because of leakage current; when the circuit is not charging and all inputs are held at some logic level, power consumption occurs. But at high frequency in switching action, dynamic power consumption contributes to overall power consumption. A capacitive charging and discharging output load dynamic power consumption is raised even more.

Static and Dynamic power are two the main sources of power dissipation in modern very large-scale integration (VLSI) circuits, namely the dynamic in VLSI circuits [5]. Dynamic power is consumed when the signals change their states from low to high or *vice versa*, and the device is in active mode when it consumes dynamic power. Static When the device is turned ON, static power is consumed, but in standby mode, no input changes.

Power consumption in CMOS devices includes four components dynamic power, short circuit power, leakage power and static power. Maximum power is contributed by dynamic power, and short circuit power takes second place, whereas static power is when the device is under standby mode.

Sources of Leakage Currents

The leakage current consists of six current parameters in deep submicron transistors. Fig. (**1**) shows current leakage parameters.

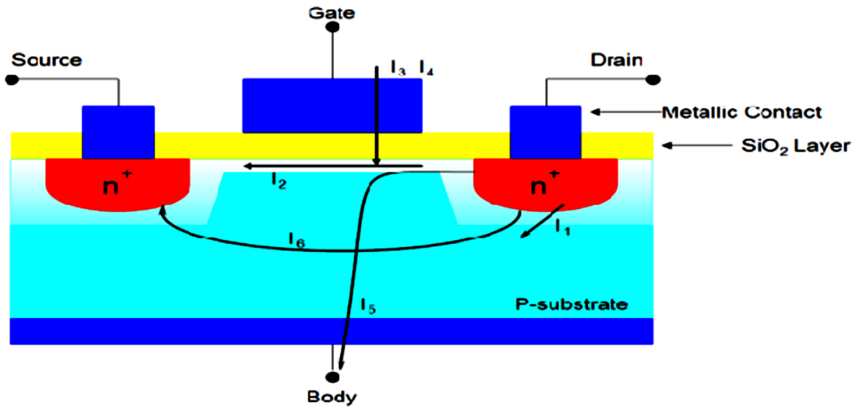

Fig. (1). Current leakage parameters.

SUBJECT INDEX

A

B

C

D

E

F

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Q

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W

Z

Ekta Goel

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