MULTISTAGE INTERCONNECTION NETWORK DESIGN FOR ENGINEERS

Shilpa Gupta

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Multistage Interconnection Network Design for Engineers

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PREFACE

In order to meet the demanding needs of ever-increasingly computationally intensive applications, such as SCADA, power distribution and management with prior load prediction, plasma dynamics for fusion energy applications, electronic structure calculations for the design of new materials and their characterization, fluid dynamics, the study of turbine behavior for electricity generator, weather prediction, and global climate change, military surveillance, symbolic computations, data mining for modeling business and financial processes, ocean sciences, enhanced oil and gas recovery, airbus design, nuclear weapon detonation, etc., Big Data Analysis must be conducted for these applications from several nodes dispersed across various locations. Fast calculation and communication are needed for this big data, which are made possible by the numerous processors connected to supercomputers.

The implementation of the switching fabric of high-capacity communication processors, such as ATM switches, gigabit Ethernet switches, and terabit routers, is also becoming more commonplace. MINs are frequently used in the context of SIMD (single-instruction multiple-data) and MIMD (multiple-instruction multiple-data) parallel machines. For instance, the nodes of the CARY X-MP and IBMSP series are typically connected using MINs. Real-world examples of practical applications that use MINs for communication include ATM Switches, the Butterfly parallel processor, the IBM SP series, the IBM research prototype RP3, AMD64, SPARC, MIPS, PA-RISC, Alpha, STARAN by Goodyear Aerospace Corporation, Ethernet switches and routers, IBM Power microprocessors, and the NYU ultra-computer.

The interconnection of these supercomputers' component parts, such as the processor and their memory modules, is crucial for the reliable operation of the system. Multistage Interconnection Networks (MIN) are typically used as interconnection systems for these frameworks due to the growing number of processors in supercomputer systems. MINs consist of multiple stages of a small interconnection network known as SE connected in a predefined connection pattern. MIN provides a compromise between a highly efficient and expensive crossbar network and a bus network, which is very cost-effective but at the same time, it provides data communication at very slow rates. MIN not only provides efficient communication at low cost but it also offers high fault tolerance capability, availability of multiple paths, high bandwidth, throughput, etc. Therefore, since MIN's development, researchers have been quite interested in finding ways to improve its reliability.

A lot of designs based on regular (uniform connection pattern between stages and a number of Switching Elements (SE) are also the same in each stage) and irregular (non-uniform connection pattern between stages and number of SE are also not same in each stage) MIN topologies have been proposed in the last five decades. During the last three decades, regular rectangular (number of input and output nodes are same) MIN, primarily the Gamma Interconnection Network (GIN) and the Shuffle Exchange Network (SEN), by offering numerous routes between each Source-Destination (SD) node pair, have been investigated and improved. The majority of the improvements were made by adding more hardware (either by expanding the size or quantity of SE per stage or by expanding the number of stages). Despite the fact that SEN and GIN have received a lot of attention, there are following points that need to be highlighted. (i) Literature on these topics lacks organization and classification; (ii) certain aspects, such as complexity, cost, the number of disjoint pathways under the assumption that the source and destination are fault-free, low latency, high bandwidth and throughput, CPU usage, etc., remain to be investigated; (iii) hardware reduction (number of

SE/Stages); (iv) less research has been done on all three reliability evaluation metrics, including fault tolerance, network reliability (NR), broadcast reliability (BR), and terminal reliability (TR), for networks larger than 8×8.

In this book, these issues have been discussed and resolved by presenting the (i) Classification of SEN and GIN, (ii) A method based on using MUX and DEMUX of various sizes such as 2×1/1×2, 4×1/1×4 etc. at input and output stages respectively; (iii) Suggestions on connection patterns for MUX and DEMUX at input and output stages, respectively and (iv) design of MIN with fewer stages and more entirely isolated pathways.

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CHAPTER 1

Multistage Interconnection Networks: Introduction

Abstract: Tremendous advancements have been reported in the computer and communication industries due to the high demands of big data analysis. This led to the use of parallel and distributed processors to play a part. These parallel processors have to be connected to a large number of memory modules. The connection between these processors and memory modules must be highly reliable for efficient big data analysis. Multistage interconnection networks (MIN) provide data communication between processors and memory modules at efficient speed with reasonably high reliability. This chapter provides a detailed introduction to MINs with their evolution and characterization. Further in this chapter, the research trends among researchers about various classes of MINs have also been discussed.

Keywords: Multistage Interconnection Networks, A Switching Element, Processor Element, Shuffle Exchange Network, Gamma Network.

1.1. HISTORY AND EVOLUTION

Since the inception of Integrated Circuits (ICs) in 1959, there is a phenomenal growth in the field of VLSI technology in the form of computer and communication technologies [1-12]. To fulfill the demanding specifications of continuously increasing computational intensive applications such as power management at the substations and their load predictions, database management, and data mining, controlling and analyzing nuclear fusion reactions, characterization of materials at micro and nanoscale, fluid dynamics, weather prediction, navigation for security purpose and military surveillance, ocean sciences, advanced graphics and virtual reality, refineries, the detonation of nuclear weapons, quantum mechanics, networked videos and multimedia technologies, cryptanalysis, medical imaging and diagnosis *etc*., it is necessary to process efficiently at a very fast rate. [1-3, 5]. Though at present, computations of the order of Tera-Flops are feasible but the applications also have increased phenomenally in terms of computations requirement, and ultra-high speed is the need of the day. To cope with these technological advancements, higher transmission rates are needed with efficient processing, which are made amenable by using multiple processors connected in parallel and are termed as parallel or

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distributed systems [6, 8]. These parallel or distributed systems can be characterized into three different classes; these are:

i. Pipelined computers
ii. Array processors
iii. Multiprocessor systems

In pipelined computers, the instructions are executed in an overlap fashion, whereas, array processors consist of a processing element (PE), a control unit (CU) and an interconnection network (IN). CU broadcasts the set of instructions to all PEs and PEs execute these instructions in a lock-set-up fashion, whereas IN is a communication network that communicates data between PEs and their respective memory modules. Array processors are also known as SIMD machine which performs the computation of array or matrices of data streams [7, 8, 12].

A multiprocessor system is a computer consisting of multiprocessors with their shared or individual memory modules. A single integrated operating system controls all the processors connected through an interconnection network in multiprocessing systems. These processors asynchronously or autonomously execute different instructions on different data and are considered as MIMD machines [2, 6, 9]. Multiprocessing systems can further be classified into two groups:

i. Loosely coupled multiprocessing systems
ii. Tightly coupled multiprocessing systems.

Loosely coupled multiprocessing systems: also known as distributed systems. In these systems, processing elements contain their own memory modules as well as I/O devices (local memory modules and I/O devices). These elements communicate through interconnection networks. Most of the data in these systems is accessed from its own local memory.

Tightly coupled multiprocessing system: In these systems, PEs use shared memory modules, although, each PE may contain small local memory in the form of a small cache. INs are used to provide communication paths between all PEs with their shared memory modules and I/O devices [3] in these systems as well.

Fig. (**1**) shows the classification of parallel computer systems and Fig. (**2**) shows the configuration of loosely coupled and tightly coupled systems.

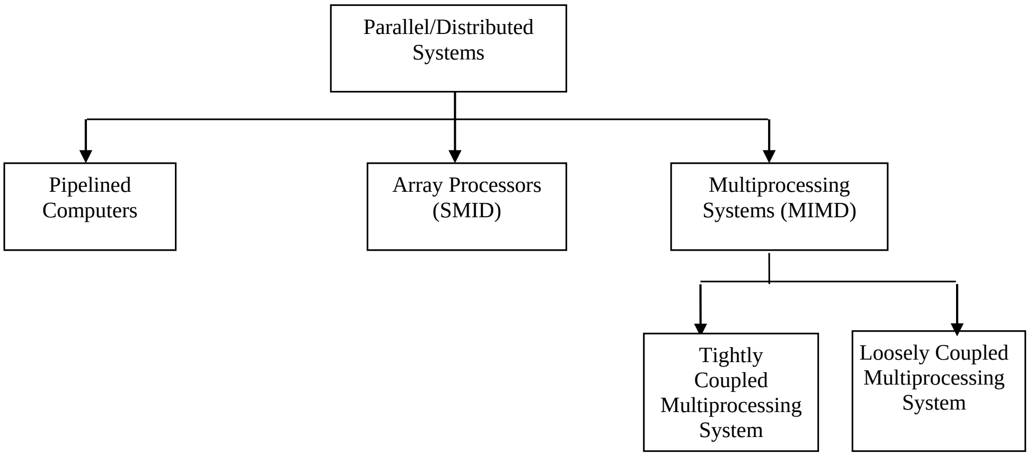

Fig. (1). Classification of Parallel/ Distributed computing system.

During the continuous research in parallel and distributed computing systems, researcher were attracted toward finding the efficient communication media, which can communicate data packets efficiently between multiple fabricated components. INs were found as an efficient communication media for these systems [4-7].

1.2. INTERCONNECTION NETWORK

The early advancement of INs was motivated by the growing demands of the communication industry such as telephone switching. But with the growth of the computer industry and the advent of fast packet-switching networks, the application of INs became apparent. Early INs for parallel processing have now found application in fast packet-switching designs [8]. The need for fabricating hundreds and thousands of PEs on a single chip came into play where crossbars became a bottleneck. Researchers started considering the possibility to find cost-effective communication media which can connect thousands of processors to their respective memory modules [9]. In the early 70s, a network consisting of small cross-bar switches *i.e.* Switching Elements (SEs) connected in multiple stages was fabricated on a single chip to provide communication between each source and the desired destination, known as Multistage interconnection Networks (MINs) [1-8]. MINs had become a favorite choice for multiple/distributed processing systems due to their fault tolerance capability, multipath availability, cost-effectiveness, *etc*. [13-20]. From the early 80s, the majority of research has reported improvements or development in these types of MINs to provide communication through more number of paths with increased fault tolerance and

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CHAPTER 2

Evolution of Fault Tolerant SEN MIN

Abstract: The shuffle exchange network is known to be the simplest MIN with a modest size of switching element in use. It is a unique path MIN with no fault tolerance. Researchers have explored this network to take advantage of its modest size and low cost and tried to improve its reliability by providing redundancy in its basic structure. While improving the fault tolerance of this network, many techniques have been proposed in the literature which are comprised of increasing the hardware complexity of the network. Recently, a new method has been proposed to improve fault tolerance which consists of using multiplexers and demultiplexers at the input and output stages of the network. It has been claimed that it improves the reliability on one hand and reduces the overall cost of the network on the other hand. In this chapter, this technique has been explored and reliability analysis of the network has been presented thoroughly to provide deep insight into the performance of the network.

Keywords: Demultiplexers, Fault Tolerance, Multiplexers, Reliability, Shuffle Exchange Network, SEN-Minus.

2.1. INTRODUCTION

High performance computer are continuously being demands as they find applications in various fields and technology such as:

- Semiconductor technology
- Power distribution, power management and load prediction
- Study of turbine behavior for electricity generator
- Communication system and technology and IoT
- Weather forecasting
- Under sea surveillance for safety and precise communication
- Electronic structure design and calculations
- Nuclear fusion and nuclear reactor design
- Material and structural analysis

Although high-performance processors have been introduced into the market with increased speed, almost doubling every three years [18], even this is not enough to meet present day processing demands. To meet such requirements, parallel proce-

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ssors came into the picture, which can be interconnected with memory modules through MIN. Hence, designing ultra-high reliable and cost-effective multipath MIN is both a critical and challenging task for network designers.

Shuffle Exchange Network (SEN) is known to be a probable MIN because it uses a regular topology with a modest size of 2×2 Switching Element (SE), which is known to be the smallest SE available. But fault tolerance is an issue in SEN, as it possesses a single path between each source to every destination. Many networks have been introduced in the past to increase fault tolerance in the SEN such as SEN+1, SEN+2, SHSEN, EGN, IEGN and Pars . It has been observed that most of these networks provide fault tolerance at intermediate stages only and very few studies exist which present a method of providing fault tolerance at input as well as output nodes. Also, the methods that exist in the literature provide fault tolerance at the cost of increased hardware for a given network topology. Fewer efforts have been made to reduce the hardware in terms of the number of SEs utilized in the network topology. A new network named SEN-Minus has been explored, which incorporates features of fault tolerance with improved disjoint paths, thus improving the reliability of the entire network.

2.1.1. Preliminaries and Background

The proposed topologies of MIN at early stages incorporated small cross-bar switches which had been organized in different stages. Since then many new design architectures have been proposed based on MIN topology in the last five decades. The first MIN network, named as Clos network, was introduced in 1953 by Charles Clos [28]. In this network, it has '3' stages: the first stage of the network consisted of *'r'* switches, with switch size $s \times t$. The middle stage had *'t'* switches of size $r \times r$ each, and the last stage is the same as that of the first stage. Thus, the network has 'N' terminals at the input and 'N' terminals at the output stage, where *'N' = r × n (number of SEs × number of input/output ports in each switch)*. The architectural topology of many MINs in the existing literature is usually comprised of *2×2* fully-crossbar switches with *'n'* number of stages, where *'n'*$=\log_2 N$. There are total *'N/2'* SEs in each stage. Hence for a network of size '*N×N',* the total number of switches used in the network is *'N/2* $(\log_2 N)$*'* and its cost is moderately small as compared to fully-crossbar networks, where the cost of a fully cross-bar network for the same number of input and output port will be 'N^2'. Regular networks also known as square networks, maintain uniform connection patterns between stages and possess unique/multiple paths between each S-D node pair. These networks in the literature exist with different names mentioned as under:

1. Delta Network [15, 18, 29, 30]
2. PM2^i Network [8, 10, 21 - 24, 72, 76]
3. Clos Network [16, 17, 19, 25, 28]
4. Cube Network [98]
5. Benes Network *etc*. [1]

Larger-sized SE, other than 2×2 *SE,* has also been used in some of the networks to provide either reduction in the number of stages, which may reduce the latency offered by the network, or to provide redundancy in the network by increasing the number of alternative paths and hence, enhancing fault tolerance. Many new network topologies have been proposed to provide improved redundancy in its structure in different ways. On the basis of a comprehensive study of these MINs, it has been found that many improvements which have been incorporated to increase their redundancy are based on adding extra hardware to the structure in different ways. These methods have been mentioned below by which the redundancy has been improved:

1. Adding extra stages of SEs to the network [45 - 46, 51,77, 84, 87, 98, 107].
2. Varying the size of SEs [15, 47, 50, 62 - 63, 65, 75, 78-82, 89, 100, 105].
3. Adding extra links to the network in between stages [81 - 82].
4. Adding extra groups consisting of SEs in the overall network [41, 42, 46].
5. Adding replicated layers [49, 83, 103, 105 - 108].
6. Modifying regular/irregular network into irregular network [31, 47].
7. Introducing intra-stage looping within the same stage [105 - 108].

2.2. SHUFFLE EXCHANGE NETWORK (SEN)

Network with Perfect Shuffle was first introduced by H. S. Stone [29] in 1971 and Delta networks were introduced by Patel [18] in 1981 and it has the property of digit controlled routing, which means that a path can be setup through the network in a distributed manner by using each binary bits of the destination address. A further generalization of Delta Networks, called Generalized Shuffle-Exchange Network (GSN) was introduced by Bhuyan and Agarwal [30] in the year 1983.

Shuffle Exchange Network (SEN) is the main member of Delta class of network and has been considered a potential candidate as MIN because of its simplest structure and topological quality with other topologies of the same class. SEN is a unique/single path regular MIN and does not possess any fault tolerance in its basic structure. Much research has been done in the recent past to enhance fault tolerance of SEN MIN by incorporating many changes in is topology and based on which, several new topologies have been developed belonging to the same

CHAPTER 3

Evolution of Gamma-Minus MIN

Abstract: Gamma interconnection network is a fault-tolerant MIN with multipath characteristics. Even though the gamma interconnection network has a multipath between every source and every destination, it has the critical flaw of acting as a single path MIN when the source address and destination address are the same. Hence, it is important to modify such a prominent candidate so as to provide multiple paths in every case, several modifications have been suggested by the researchers in the literature. One such modification is fascinating as it provides multiple paths for every case at a reduced cost. At the input and output stages, multiplexers and demultiplexers are used to do this. The system is referred to as Gamma-Minus MIN. This chapter includes further performance characteristics with the reliability assessment of Gamma-Minus MIN.

Keywords: Fault tolerance, Gamma-Minus, Reliability, Tag Value.

3.1. INTRODUCTION

Due to their good fault tolerance capability, gamma networks have been proposed as a viable choice for supercomputer systems. It is a multipath MIN that uses SE of size 3×3 for network size “N” in its fundamental topology. It has a total of 'n' stages where ‘$n = \log_2 N$’ and each stage comprises ‘N’ number of SEs.

Despite being a multipath MIN, Gamma MIN has the significant drawback of being a unique path when the source and destination terminals have the same address. Extensive research has been done and many modifications/improvements have been suggested and implemented on Gamma MINs and several new topologies of the same class have been in literature [20 - 25, 63-68, 72, 74-95, 101-102]. The modifications suggested in the literature are listed as:

i. **Added number of stages:** Extra Stage Gamma (EGIN) [87], Incomplete Gamma Interconnection Network (IGIN) [84], Incomplete Cyclic Gamma interconnection Network (ICGIN) [84], *etc*.

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i. **Modifying existing connection patterns of GIN:** Balanced Gamma (BGIN) [83, 88], Modified Balanced Gamma (MBGIN) [80], Cyclic Gamma (CGIN) [21, 74], Mono-Gamma Interconnection Network (MGIN) [21, 74] Reliable Gamma (REGIN) [75], Non-backtracking Gamma (NBGIN) [78], *etc*.
ii. **Increasing the size of SE:** 3-Disjoint Gamma (3D-GIN) [81], 4-Disjoint Gamma (4D-GIN) [63], Fault Tolerant Interconnection network (FTIN) [65], Enhanced Inverse Augmented Data Manipulator (EIADM) [81], Improved Enhanced Augmented Data Manipulator (IEADM) [102] and Improved Logical Neighborhood Network (ILN) [102], Minimal Links Traversed Dynamic Rerouting with Extra Link at Initial Stage (MINGIN-1) and Minimal Links Traversed Dynamic Rerouting [90, 91], *etc*.
iii. **Providing intra-stage chaining:** Partially Chained Gamma Interconnection Network (PCGIN) [79], Fully Chained Interconnection Network (FCGIN) [79], *etc*.

From this critical and comprehensive survey conducted on Gamma MIN, some of the observations are made are summarized as:

i. Most of the attention had been paid to increasing the redundancy of the network at intermediate stages only.
ii. Most of the evaluations done in literature on Gamma MIN are restricted to TR computations only and that too for network size N = 8 and for the worst case (for tag value ‘T = 0’ where source and destination terminals have the same address).
iii. In existing lit,erature it has also been stated that EGIN has a minimum TR [77].
iv. The majority of authors in the literature currently in existence have utilized similar reliability values for SEs of various sizes, such as SE of size 1×3, 3×3, 3×1, 2×4, 4×2, 2×1, 1×2, *etc*. have assumed to have the same reliability 'r'. Hence reliability evaluation for different topologies with the assumption of identical reliability for SEs of different sizes will be erroneous.
v. Other performance metrics such as BW, throughput, processor utilization, *etc*. have not been given much consideration for existing Gamma MINs.
vi. Despite the fact that there isn't much literature on the usage of MUXs and DEMUXs at the input and output stage of MIN, there is no specified pattern suggested for connecting MUXs at the input terminal and DEMUXs at the output terminal.
vii. Several new methods have been proposed in literature to mitigate these mentioned problems and new network architecture has been proposed by the authors in literature which is explored in this chapter.

3.2. BACKGROUNDS AND PRELIMINARIES

$PM2^i$ networks, also known as Data Manipulator networks, are square multistage networks with an equal number of input/output ports. The Plus Minus 2^i ($PM2^i$) pattern is the basis for the connection pattern between successive stages, where ‘i’ is the count of stage named from ‘0’ to ‘n’. For the network size of N×N, $PM2^i$ network consists of ‘N’ number of inputs as well as outputs. It has total‘n+1’ stages, where ‘n’ = $\log_2 N$ [8, 10, 21-24, 72, 76]. 'N' SEs of having configuration 3×3 are connected at the intermediate stage of each step, while SEs with the size of 1×3 and 3×1 are coupled at the input and output stages. Each SE has three input and output terminals, where, three SEs at stage 'j' are connected to the output terminals of the SE at stage 'i' using the stated connection pattern of '$(j-2^i) \bmod N$', 'j', and '$(j+2^i) \bmod N$'. The connection pattern of 3×3 SE is shown in Fig. (**1**), GIN was introduced in 1984 [73]. Since then it has been considered in this research for analysis purpose. The classification of Gamma interconnection network is shown in Fig. (**2**).

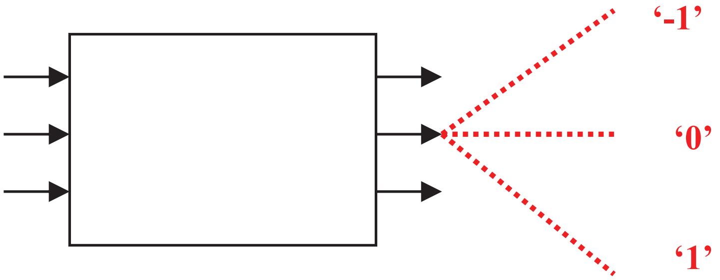

Fig. (1). Routing mechanism of 3×3 SE.

Gamma Interconnection Network (GIN): It has “N” inputs and “N” outputs and “n+1” stages ranging from 0 to n, where n can be expressed as $\log_2 N$. Except for the input and output stages, where each SE has a 1×3 and 3×1 configuration, respectively, there are N SEs of size 3×3 [20]. The pattern of connection of SEs at adjoining stages is based on $PM2^i$ pattern [20, 77, 87, 115, 120], for example for stage i^{th}, the connection pattern from ‘j^{th}’ SE will be ‘$j \pm 2^i$’. The gamma network's design is shown in Fig. (**3**) With the exception of the tag value “0,” which occurs when the source (S_i) and destination (D_i) are the same ($S_i = D_i$), the GIN is a fault-tolerant network in its basic setup. In this case, the network operates as a single path MIN [20, 77, 87]. The amount of pathways connecting every source node to each destination node is determined by the tag value “T,” which determines how the gamma network's paths are distributed. It is described as the difference between the source and destination addresses and is demonstrated mathematically by equation (3.1):

CHAPTER 4

Design, Reliability Modeling and Evaluation of FTSM

Abstract: It has been proved that the use of multiplexers and demultiplexers of the smallest size has improved reliability to an extent but the effect of using bigger-sized MUX and DEMUX on reliability and fault tolerance must also be evaluated. In the recent past, the consequences of using higher-sized MUXs and DEMUXs have been explored and presented in this chapter. The full analysis of the size of MUXs and DEMUXs to be used so as to increase the reliability of the network to the optimum level has been presented. The analysis done on SEN MIN shows that the best size of MUXs and DEMUXs to be used is 4×1 and 1×4 respectively and hence the SEN MIN with 4×1 MUX and 1×4 DEMUX is named Fault Tolerance SEN MIN (FTSM).

Keywords: Demultiplexer (DEMUX), Fault Tolerance SEN MIN (FTSM), Multiplexer (MUX), Reliability-to-Cost (RCR) ratio, Switching Element.

4.1. INTRODUCTION

MINs provide effective communication between processors and memory modules for parallel and distributed computing systems. Though, SEN-Minus can be viewed as a potential network to manage efficient communication, fault tolerance at input and output stages is still an issue. SEN-Minus provides fault tolerance to the system at these stages, but a maximum of up to one fault can be tolerated at the input/output stage in this network. In supercomputer systems, there are thousands of processors connected in parallel along with the memory modules. Hence, there is more probability of occurrence of faulty/busy switches at input/output stages as two or more processors may ask for the same destination or memory module at the same time. For these bottlenecks, there is a need for further improving the fault tolerance of MINs at the input/output stage. A new topology has been developed to provide maximum fault tolerance at low cost and named as Fault Tolerant SEN-Minus (FTSM), which is highly reliable with maximum fault tolerance (up to '3' faults) at both input and output stages. FTSM consists of 1×4 MUXs and 4×1 DEMUXs connected at input and output stages, respectively. It has been observed that with the increasing size of MUXs and DEMUXs, reliability increases, but this improvement is limited and may not be responsive to

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large-scale systems as network complexity and cost grow with the system size. In this chapter, different topologies of SEN MINs have been explored with different sizes of MUXs and DEMUXs and their TR has been computed. The effect of the size of MUXs and DEMUXs on TR and cost has been analyzed. A new parameter namely, Reliability-Cost-Ratio (RCR), has been defined to establish conciliation between enhanced reliability and cost offered. Hence, based on the computed RCR, an optimum size of MUXs and DEMUXs which can be used with MINs has been presented.

4.2. PRELIMINARIES AND BACKGROUNDS

Different types of SEN MINs and their important features which exist in literature are given in this section. The important features of these topologies have been discussed in the subsection given below.

4.2.1. Variants and Features of SEN MIN

SEN is a single path MINs having a regular structure for the size of N × N, where 'N' is the number of inputs as well as output terminals [35, 36, 39, 40, 52, 55, 62, 64, 112]. It consists of an 'N/2' number of SEs of size 2×2 at each stage, with a total number of $\log_2 N$ stages. It offers no fault tolerance in the network. To improve its fault tolerance, many new methods have been suggested in literature such as adding an extra stage discussed below.

In SEN+1, there is one additional stage given due to which it possesses two paths between each S-D node pair. The important features of SEN+1 are: it has high reliability and fault tolerance than SEN MIN and it can tolerate one fault at intermediate stages but no fault can be tolerated at the input and output stages.

In SEN+2, there are additional stages attached due to which it possesses four paths between each S-D node pair. The important trait of SEN+2 is that it can tolerate multiple faults at intermediate stages [35 - 36, 39 - 40] but no fault tolerance is provided at the input and output stage.

Another member of the SEN family *i.e.* SHSEN (Symmetric homogeneous SEN) MIN has four paths between each S-D node pair. It comprises N number of inputs and outputs with $((\log_2 N) + 1)$ stages having a total of 'N' number of SEs at each stage [45]. The important characteristic of this network is that it possesses two disjoint paths *i.e.* it can tolerate one fault both at input and output stages, but the cost of the network is very high as the number of SE per stage is doubled.

Low-cost SEN-Minus MIN provides two totally disjoint paths which tolerate one fault at the input as well as the output stage.

In this chapter, two improved methods have been presented. The first method provides ‘4’ disjoint paths between each S-D node pair. The second method describes the effect of the size of MUXs and DEMUXs at the input and output stages of various SEN MINs on reliability. A new parameter has also been presented to evaluate reliability w.r.t. cost and disjoint paths offered by the topology. Hence, an optimum size of MUXs and DEMUXs has also been presented. The description has been discussed in the next section.

4.3. DESIGN, RELIABILITY MODELING, AND EVALUATION OF FTSM MIN

For designing highly reliable FTSM, the design [117] consideration taken is as follows:

i. 4×1 MUX and 1×4 DEMUX have been used at the input and output stages.
ii. Modification of the connection pattern has been done. Fault Tolerant SEN-Minus (FTSM) has been designed with a total of eight paths; out of which; four paths are totally disjoint (node and link disjoint) between each S-D node pair.
iii. Reliability modeling and evaluation have been done on FTSM MIN which is presented in the next section.

4.3.1. Design and Reliability Evaluation of FTSM

FTSM contains N input terminals and N output terminals with a total of ($\log_2 N$ -1) stages with N/2 SEs at each stage. It comprises N number of 4×1 MUXs and 1×4 DEMUXs at input and output stages, respectively.

This FTSM design has been implemented which results in a total of eight paths between each S-D node pair out of which four totally disjoint paths are there. Whereas, existing networks in the literature provide a maximum of four paths out of which only two paths are totally disjoint.

Routing: FTSM topology is shown in Fig. (**1**) for an 8×8 network size. There are two MUXs and DEMUXs attached to each SEs at input and output stages, out of which one is attached to all even inputs/outputs (such as ‘0’, ‘2’, ‘4’ and ‘6’) and another is attached to all odd inputs/outputs (such as ‘1’, ‘3’, ‘5’ and ‘7’). The routing of a data packet from source ‘001’ to ‘010’ has been shown with red lines in Fig. **1**. There exist four paths between these S-D node pairs and the same is applicable for all other S-D node pairs. FTSM becomes highly reliable and fault-tolerant as multiple disjoint paths are present in the network between each S-D

CHAPTER 5

Design and Reliability Modeling of FTGM

Abstract: The gamma interconnection network is a reliable network that provides redundancy in its basic topology but fault tolerance is still an issue to be addressed. Although the usage of MUX and DEMUX lessens the issue in gamma MIN's unique path behavior when the tag value is zero, it is still necessary to investigate the ideal size of MUX and DEMUX which may be used with gamma MIN in order to give the highest level of reliability. In order to make an overall generalization about all MINs, it is crucial to determine whether the findings achieved for the SEN MIN apply to other MINs that use switching elements of varying sizes. This chapter evaluates and presents the impact of larger MUX and DEMUX sizes on gamma MIN. The results of the evaluations show that the 4×1 MUX and 1×4 DEMUX provide the maximum level of dependability and that increasing the size of the MUX and DEMUX lowers the reliability to cost ratio.

Keywords: Fault-tolerant gamma-minus (FTGM) MIN, Fault tolerance, Gamma-Minus MIN, Reliability, Reliability-cost-ratio (RCR).

5.1. INTRODUCTION

MINs are crucial components of the parallel interconnection network that connects multiple processors and memory modules in the age of the supercomputer. Gamma networks are seen to have the capacity to handle effective communication, however, they still have a fault tolerance problem. Gamma-Minus networks give the system fault tolerance, however, the input and output stages can only accept one defect at a time. In systems used by supercomputers, where thousands of processors are connected in parallel, there is a higher likelihood that switches at the input, output, and intermediate (in the case of tag value “0”) stages of the network would malfunction or be overloaded. To fill this gap, there is a need for further improvement of fault tolerance of the already Gamma-Minus MIN so as to provide multi-paths (more than two paths), especially for tag value ‘0’, where there are only two paths available. Gamma MIN is also recognized as a redundant network because it offers several connections between each pair of S-D nodes (with the exception of tag value '0'). This is due to the use of N numbers of 3×3 SEs in its basic structure with a total $\log_2 N+1$ number of sages. It possesses 192 units of cost for an 8×8 sized network,

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whereas for the same network size, SEN MIN (unique path) offers 48 units of cost. Hence, it can be said Gamma MIN provides fault tolerance at a very high additional cost as compared to SEN MIN. Therefore, there is an urgent need to create a new MIN that belongs to the Gamma class at a similar price as SEN. Two novel topologies are now introduced in this chapter to offer the highest level of fault tolerance at the lowest possible cost. These two networks, Fault Tolerant Gamma-Minus-1 (FTGM-1) and Fault Tolerant Gamma-Minus-2 (FTGM-2), are extremely reliable networks with maximum fault tolerance (up to '3' faults) at input, output, and intermediate stages (particularly in case of tag value '0'). These networks offer the greatest amount of entirely disconnected paths with the shortest path lengths between each pair of S-D nodes, which mitigates the majority of the drawbacks of the current gamma topologies. FTGM-1 has the lowest cost as compared to the current gamma MINs.

5.2. BACKGROUNDS AND PRELIMINARIES

Gamma Interconnection Network (GIN) is a redundant MIN with 'N' inputs/outputs and total 'N+1' stages labeled from '0' to 'N', where '$N = \log_2 N$'. Each stage has 'N' numbers of SEs configured as a 3×3 full crossbar switch, with the exception of the input and output stages where each SE is of 1×3 and a 3×1 configuration. As mentioned in section 3.2 [20 - 21], the connection pattern of the gamma network's intermediate stages is based on $PM2^i$.

With the exception of the tag value “T = 0,” where it acts as the unique path MIN, GIN has several paths connecting each pair of S-D nodes. The literature has described a number of solutions to this issue, including:

i. Re-shuffling the connection pattern to improve fault-tolerance such as in Mono-Gamma network (MGIN) [21, 74], Cyclic Gamma network (CGIN) [21, 74], Reliable Gamma network (RIN) [62], Non-backtracking Gamma network (NBGIN) [78] and Modified Balanced Gamma network (NBGIN) [80]. To achieve numerous pathways for tag value “0,” different stages' connection patterns in these networks have been adapted.
ii. Adding more stages to the Gamma network to create various pathways. Many networks have been introduced based on this, such as EGIN [87], Incomplete GIN, and Incomplete CGIN [84].
iii. Bigger sizes of SE such as in 3-Disjoint Gamma network [81], 4-Disjoint network [63], 3D-Cyclic GIN [92], Reliable Interconnection Network (RIN-1 and RIN-2) [62], Combined Switch MIN (CSMIN), and Fault Tolerant Interconnection Network (FTIN) [65].

iv. Intra-stage chaining such as in Partially Chained CSMIN (PCGIN) and Fully Chained CSMIN (FCSMIN) [50, 82].

On the basis of review of reliability and fault tolerance capability of above mentioned MINs, some of the gaps have been found which are listed below:

1. All MINs described in literature offer partially disconnected pathways under the assumption that input and output nodes are failure-free and crucial.

2. Possessing less cost is the foremost requirement in MIN. Due to the use of SEs of size 3×3 in redundant gamma networks, it possesses high cost comparative to SEN network family.

3. Supercomputers are devices that connect thousands of processors in parallel (there are typically 2^6 to 2^{16} processors connected). MINs used for these machines should consist of higher configuration (up to the network size of 1024×1024). The probability of request generated from many processors for the same destination at one time is high, so MINs employed should be multiple fault-tolerant at input as well as output node. Not much literature is available to deal with this problem.

4. The reliability analysis is made more difficult by the fact that every gamma MIN now in use has a varied number of pathways for various tag values. Additionally, no study to far offers a full examination of the multiple reliability factors.

5. It has been noted that there are more pathways between each S-D node pair as the network gets bigger. However, most paths fail when one SE fails at the input/output stage because there is a greater interdependence between system components (SE) and the total pathways accessible as the network grows.

In today's rapidly changing environment, enhancing reliability is a constant priority in order to fulfill the demanding needs of ever evolving super systems. In order to close the gaps, two new designs that are both economical and feature a higher number of entirely disconnected paths with shorter paths connecting each S-D node pair have been analysed and studied in this chapter. In the following section, the techniques mentioned based on which these highly reliable multiple fault tolerant networks known as FTGM-1 and FTGM-2 are a part of the gamma MINs are discussed.

5.3. DESIGN AND RELIABILITY OF FTGM-1 AND FTGM-2

The following are the steps involved in designing the FTGM-1 and FTGM-2 [121] topologies:

CHAPTER 6

Design and Reliability Evaluation of SEGIN-Minus

Abstract: It has been shown in the previous chapters that SEN and gamma interconnection network are the best-known MIN and are highly explored in the literature. It would be interesting to make a hybrid network comprising combined characteristics of both networks. Few research works are available in the literature which have explored this interesting topic and reliability evaluations have also been presented. These networks are known as SEGIN and SEGIN-Minus MIN. In this chapter, detailed reliability analyses of both networks have been presented and it is shown that SEGIN-Minus MIN has better performance characteristics than the SEGIN network.

Keywords: Fault tolerance, Reliability, Shuffle exchange gamma interconnection network (SEGIN), Shuffle exchange gamma-minus interconnection network (SEGIN-Minus).

6.1. INTRODUCTION

Computational intensive applications such as navigation, power generation and distribution, weather forecasting, telemetry, Iot, cloud computing, *etc*. need high computational power. To achieve these highly computational-efficient systems, multiple processors must be connected in parallel along with the required memory modules. To connect these parallel processors with memory modules, MINs are used, which provide programmable data paths between connected modules, at a reasonable cost. SEN and Gamma MINs have been studied extensively in the literature [41 - 47, 49-51, 63-63, 65, 75, 77-82, 84, 89, 98, 100, 105-111]. SENs are known to have an uncomplicated/regular structure and easy control routing, whereas, GIN produces more number of paths for each S-D node pair. A lot of research has been undertaken in the last decade, by the keen researchers to make MINs more redundant. A new approach has been introduced in recent past [111] in which SEN and GIN MINs have been recombined to form new network, namely, Shuffle Exchange Gamma Interconnection Networks (SEGIN) which provides several paths between each Source-Destination (S-D) node pair. A hybrid SEGIN has been obtained and acclaimed to have reliability better than both GIN and SEN and their respective variants of equal size. It has also been acc-

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laimed that the hardware cost of SEGINs is lower than that of GINs and almost equal or slightly higher than that of SEN and its variants. Though, in this chapter, it has been found that SEGIN (for 8×8 network size and '4' stages) has more number of stages as compared to SEN-Minus (for 8×8 network size '2' stages) and GIN-Minus (for 8×8 network size '3' stages) MINs. Also, the structure does not possess fault tolerance at input and output stages and it has been assumed as the SEs at these stages are critical and are failure free. The reliability, which has been assumed to be increased, has only been increased by approximately 8% w.r.t. SEN and GIN MIN. although the increment in the cost of SEGIN MIN w.r.t. SEN MIN is approximately 66%. A new network is presented in this chapter to address the above mentioned reliability issue w.r.t. cost of the network with the introduction of totally disjoint paths (node and link disjoint). To assure that reliability has been improved and increased, a thorough comparison of performance measures such as reliability, fault tolerance, cost, *etc*. has been shown with existing SEN, GIN and SEGIN MINs.

6.2. PRELIMINARIES AND BACKGROUNDS

Shuffle Exchange Gamma Interconnection Networks (SEGIN) consist of total 'n + 1' stages which may be numbered from stage 0 to n ('n' = $\log_2 N$, for 'N' input/output terminals) with N/2 SEs per stage. At input as well as at output stages, SEGIN utilizes a shuffle exchange pattern same as that of SEN MIN with SEs of size 2 × 2. At intermediate stages, SEs of size 2 × 3 and 3 × 2 are used in SEGIN. For these stages, the '$\pm 2^{i}$' ($PM2^{i}$) connection pattern is used which is the same as in case of the connection pattern between 0^{th} stage to 1^{st} stage of GIN and its variants. The pattern is such that j^{th} switch having of 3 outgoing links will connect as: (a) if the destination address bit for that stage consists of '0', then a straight link will be connected to j^{th} SE j in the next stage; (b) if the destination address bit for that stage consists of '-1', an upward link will be connected to $(j-1)^{th}$ SE and (c) if the destination address bit for that stage consists of '1', a downward link will be connected to $(j+1)^{th}$ SE. The four-stage design of SEGIN for N = 8 is shown in Fig. (**1**).

Although the approach is interesting, some limitations of this design have been identified and are summarized as follows:

a. More number of stages are used than SEN MIN, hence, a costlier network.
b. Reliability values for different sizes of SEs (2×2, 3×2 and 2×3) have been assumed equal.
c. Most of the calculations suggested for network size 8×8. Although, practically bigger sizes of MINs are evaluated and used.

d. The transmission path length of SEGIN is more as compared to SEN MIN.
e. Validation of evaluated values of reliability of SEGIN has been carried out by comparing it with MINs proposed in 70s or 80s. Though many new networks and improved topologies have been suggested in the last 20 years, the results of those topologies have been totally ignored which may prove themselves to be more reliable than SEGIN.

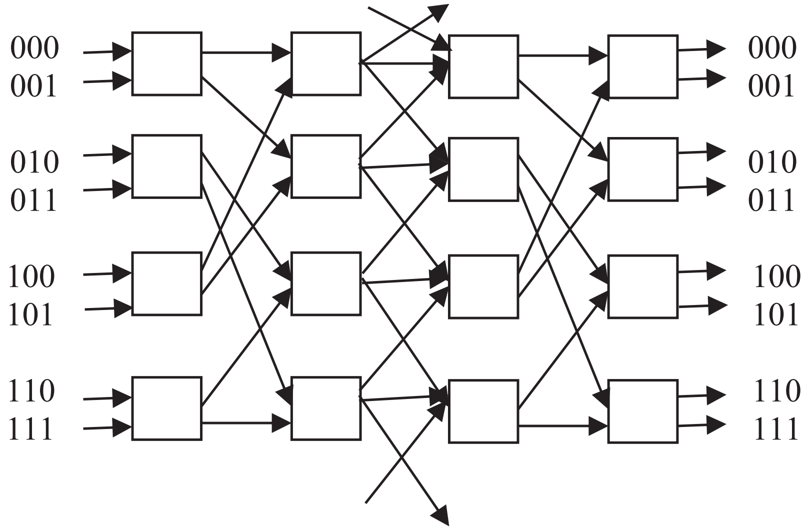

Fig. (1). Shuffle Exchange Gamma Interconnection Network (SEGIN) topology.

To mitigate these problems, a new network SEGIN-Minus has been developed recently and presented in this chapter, which provides high reliability and fault tolerance at a reasonably less cost and reduced path length. The topology of SEGIN-Minus has been discussed in detail in the succeeding section.

6.3. DESIGN AND RELIABILITY EVALUATION OF SEGIN-MINUS MIN

Combining features of SEN and Gamma MIN [122]:

a. Properties of SEN-Minus and Gamma-Minus networks have been combined to form a new topology named as SEGIN-Minus.
b. All performance metrics such as: TR, BR, NR, Cost, *etc*. have been evaluated.
c. These performance parameters have been evaluated for larger size networks (8×8 to 1024 ×1024) and compared with computed values of other SEN and Gamma MIN having 3 or more number of stages.

Reliability of SEGIN has also been recomputed by assuming true reliabilities of all SEs of different size. All reliability measures of SEGIN-Minus have been

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List of Acronyms

IN = Interconnection Network
MIN = Multistage Interconnection Network
PE = Processing Element
SE = Switching Element
TR = Terminal Reliability
BR = Broadcast Reliability
NR = Network Reliability
CE = Cost Effectiveness
BW = Bandwidth
Thru = Throughput
PA = Probability of Acceptance
PU = Processor Utilization
SEN = Shuffle Exchange Network
SEN+1 = Shuffle Exchange Network with one Extra Stage
SEN+2 = Shuffle Exchange Network with two Extra Stage
SHSEN = Symmetric Homogeneous Shuffle Exchange Network
SEN- = Shuffle Exchange Network-Minus
ASEN = Augmented Shuffle Exchange Network
EGN = Extra Group Network
IEGN = Improved Extra Group Network
PARS = PARS
E-ASEN = Enhanced Augmented Shuffle Exchange Network
RSEN = Replicated Shuffle Exchange Network
R-ASEN = Replicated Augmented Shuffle Exchange Network
R-EASEN = Replicated Enhanced Augmented Shuffle Exchange Network
SEGIN = Shuffle Exchange Gamma Interconnection Network
GIN = Gamma Interconnection Network
EGIN = Extra Stage Gamma Interconnection Network
CGIN = Cyclic Gamma Network
MGIN = Mono-Gamma Network
BGIN = Balanced Gamma Network
ReGIN = Reliable Gamma Network

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Incomplete GIN = Incomplete Gamma Network

Incomplete CGIN = Incomplete Cyclic Gamma Network

NBGIN = No Backtracking Gamma Network

Modified BGIN = Modified balanced Gamma Network

RIN-1 = Reliable Interconnection Network-1

RIN-2 = Reliable Interconnection Network-2

3DCGIN = 3-Disjoint Cyclic Gamma Network

3DGIN = 3-Disjoint Gamma Network

4DGIN-1 = 4-Disjoint Gamma Network-1

4DGIN-2 = 4-Disjoint Gamma Network-2

CSMIN / CSGIN = Combined Switch MIN / GIN

CSMINMD = Combined Switch MIN MUX DEMUX

FCSMIN = Fully-Chained Combining Switches MIN

PCGIN = Partially chained Gamma Network

FCGIN = Fully chained Gamma Network

EIADM = Enhanced Inverse Augmented data Manipulator

FTIN = Fault Tolerant Interconnection Network

MINGIN 1 = Minimal Links Traversed Dynamic Rerouting-1

MINGIN 2 = Minimal Links Traversed Dynamic Rerouting-2

DRGIN = Dynamic Rerouting GIN

B-Network = Backward Network

DR Network = Dynamic Rerouting Network

ILN = Improved logical Neighborhood network

IEADM = Improved Enhanced Augmented data Manipulator

FTIN = Fault Tolerant Interconnection Network

MINGIN 1 = Minimal Links Traversed Dynamic Rerouting-1

MINGIN 2 = Minimal Links Traversed Dynamic Rerouting-2

S-D = Source-Destination

I/O = Input/ Output

N/W = Network

List of Symbols

N = Size of Network
n = Number of Stages
r = System Reliability
RSE = Switch Element Reliability
λ = Failure Rate
RT = Terminal Reliability
RB = Broadcast Reliability
RN = Network Reliability
PO = Initial Probability
Pu = Processor Utilization
i = Switching Element number
j = Stage number

APPENDIX-A

Table A.1. Fault Tolerance Information for the various Gamma Networks (Fault tolerance criteria used is FULL ACCESS).

Network	Name of Network	Refs	Year	Fault Tolerance method	One Fault tolerant	Multiple fault tolerant	Routing scheme used
GIN	Gamma Interconnection Network	[20]	1984	Use of 3×3full cross bar Switch SE	No	No	Distance tag routing
EGIN	Extra Stage Gamma Interconnection Network	[77, 87]	1988	Providing Extra Stage	Yes	No	Distance tag routing
CGIN	Cyclic Gamma Network	[21, 74]	1994	Changing Interconnection Pattern	Yes	No	Distance, Destination tag routing
MGIN	Mono-Gamma Network	[21]	1996	Changing Interconnection Pattern	Yes	No	Distance tag routing
BGIN	Balanced Gamma Network	[88]	2006	Providing Extra Link	Yes	Yes	Distance tag routing
ReGIN	Reliable Gamma Network	[75]	1993	Changing Interconnection Pattern	Yes	No	Distance tag routing
Incomplete GIN	Incomplete Gamma Network	[84]	2013	Providing Extra Stage	Yes	Yes	Twin tag routing based on distance tag routing
Incomplete CGIN	Incomplete Cyclic Gamma Network	[84]	2013	Providing Extra Stage	Yes	Yes	Twin tag routing based on distance tag routing
NBGIN	No Backtracking Gamma Network	[78]	2001	Combining the switching elements	Yes	Yes	Destination tag routing
Modified BGIN	Modified balanced Gamma Network	[80]	1998	Changing Interconnection Pattern	Yes	No	Destination tag routing
RIN-1	Reliable Interconnection Network-1	[62]	2015	More links are used	Yes	Yes	Dynamic Routing

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(Table A.1) cont.....

Network	Name of Network	Refs	Year	Fault Tolerance method	One Fault tolerant	Multiple fault tolerant	Routing scheme used
RIN-2	Reliable Interconnection Network-2	[62]	2015	More links are used	Yes	Yes	Dynamic Routing
3DCGIN	3-Disjoint Cyclic Gamma Network	[93]	2012	Providing alternate source	Yes	Yes	Distance tag routing
3DGIN	3-Disjoint Gamma Network	[81]	2003	Combining the switching elements	Yes	Yes	Distance tag routing
4DGIN-1	4-Disjoint Gamma Network-1	[63]	2014	Combining the switching elements	Yes	Yes	Distance tag routing
4DGIN-2	4-Disjoint Gamma Network-2	[63]	2014	Combining the switching elements	Yes	Yes	Distance tag routing
CSMIN / CSGIN	Combined Switch MIN / GIN	[50, 82]	2005	Combining the switching elements	Yes	Yes	Distance / Dynamic tag routing
CSMINMD	Combined Switch MIN MUX DEMUX	[50]	2011	Combining the switching elements	Yes	Yes	Distance / Dynamic tag routing
FCSMIN	Fully-Chained Combining Switches MIN	[50]	2011	Combining the switching elements providing Extra Links	Yes	Yes	Destination tag routing
PCGIN	Partially chained Gamma Network	[51]	2000	Providing Extra Link	Yes	No	Distance tag routing
FCGIN	Fully chained Gamma Network	[51]	2000	Providing Extra Link	Yes	Yes	Distance tag routing
EIADM	Enhanced Inverse Augmented data Manipulator	[81]	2003	Completing inherent partial redundancy	Yes	Yes	Destination tag Routing
FTIN	Fault Tolerant Interconnection Network	[65]	2015	More links and Dynamic Rerouting is used	Yes	Yes	Dynamic Routing
MINGIN 1	Minimal Links Traversed Dynamic Rerouting-1	[90]	2004	Providing Extra Link	Yes	Yes	Distance tag routing
MINGIN 2	Minimal Links Traversed Dynamic Rerouting-2	[90]	2004	Providing Extra Link	Yes	Yes	Distance tag routing

(Table A.1) cont.....

Network	Name of Network	Refs	Year	Fault Tolerance method	One Fault tolerant	Multiple fault tolerant	Routing scheme used
DRGIN	Dynamic Rerouting GIN	[90]	2004	Increasing the number of network ports slightly	Yes	No	Distance, Destination tag routing
B-Network	Backward Network	[89]	1990	Providing back links	Yes	Yes	Distance routing
DR Network	Dynamic Rerouting Network	[102]	2014	Increasing the number of network ports slightly	No	No	Dynamic Rerouting
ILN	Improved logical Neighborhood network	[102]	2014	Completing inherent partial redundancy	Yes	Yes	Dynamic Rerouting
IEADM	Improved Enhanced Augmented data Manipulator	[102]	2014	Completing inherent partial redundancy	Yes	Yes	Dynamic Routing

Table A.2. Various Gamma Interconnection Network Topology for 8×8 network size.

Network	Name of Network	Ref	Year	Fault Tolerance method	One Fault tolerant	Multiple fault tolerant	Routing scheme used
GIN	Gamma Interconnection Network	[20]	1984	Use of 3×3full cross bar Switch SE	No	No	Distance tag routing
EGIN	Extra Stage Gamma Interconnection Network	[77, 87]	1988	Providing Extra Stage	Yes	No	Distance tag routing
CGIN	Cyclic Gamma Network	[21, 74]	1994	Changing Interconnection Pattern	Yes	No	Distance, Destination tag routing
MGIN	Mono-Gamma Network	[21]	1996	Changing Interconnection Pattern	Yes	No	Distance tag routing
BGIN	Balanced Gamma Network	[88]	2006	Providing Extra Link	Yes	Yes	Distance tag routing
ReGIN	Reliable Gamma Network	[75]	1993	Changing Interconnection Pattern	Yes	No	Distance tag routing

(Table A.2) cont.....

Network	Name of Network	Ref	Year	Fault Tolerance method	One Fault tolerant	Multiple fault tolerant	Routing scheme used
Incomplete GIN	Incomplete Gamma Network	[84]	2013	Providing Extra Stage	Yes	Yes	Twin tag routing based on distance tag routing
Incomplete CGIN	Incomplete Cyclic Gamma Network	[84]	2013	Providing Extra Stage	Yes	Yes	Twin tag routing based on distance tag routing
NBGIN	No Backtracking Gamma Network	[78]	2001	Combining the switching elements	Yes	Yes	Destination tag routing
Modified BGIN	Modified balanced Gamma Network	[80]	1998	Changing Interconnection Pattern	Yes	No	Destination tag routing
RIN-1	Reliable Interconnection Network-1	[62]	2015	More links are used	Yes	Yes	Dynamic Routing
RIN-2	Reliable Interconnection Network-2	[62]	2015	More links are used	Yes	Yes	Dynamic Routing
3DCGIN	3-Disjoint Cyclic Gamma Network	[93]	2012	Providing alternate source	Yes	Yes	Distance tag routing
3DGIN	3-Disjoint Gamma Network	[81]	2003	Combining the switching elements	Yes	Yes	Distance tag routing
4DGIN-1	4-Disjoint Gamma Network-1	[63]	2014	Combining the switching elements	Yes	Yes	Distance tag routing
4DGIN-2	4-Disjoint Gamma Network-2	[63]	2014	Combining the switching elements	Yes	Yes	Distance tag routing
CSMIN / CSGIN	Combined Switch MIN / GIN	[50, 82]	2005	Combining the switching elements	Yes	Yes	Distance / Dynamic tag routing
CSMINMD	Combined Switch MIN MUX DEMUX	[50]	2011	Combining the switching elements	Yes	Yes	Distance / Dynamic tag routing
FCSMIN	Fully-Chained Combining Switches MIN	[50]	2011	Combining the switching elements providing Extra Links	Yes	Yes	Destination tag routing
PCGIN	Partially chained Gamma Network	[51]	2000	Providing Extra Link	Yes	No	Distance tag routing

(Table A.2) cont.....

Network	Name of Network	Ref	Year	Fault Tolerance method	One Fault tolerant	Multiple fault tolerant	Routing scheme used
FCGIN	Fully chained Gamma Network	[51]	2000	Providing Extra Link	Yes	Yes	Distance tag routing
EIADM	Enhanced Inverse Augmented data Manipulator	[81]	2003	Completing inherent partial redundancy	Yes	Yes	Destination tag Routing
FTIN	Fault Tolerant Interconnection Network	[65]	2015	More links and Dynamic Rerouting is used	Yes	Yes	Dynamic Routing
MINGIN 1	Minimal Links Traversed Dynamic Rerouting-1	[90]	2004	Providing Extra Link	Yes	Yes	Distance tag routing
MINGIN 2	Minimal Links Traversed Dynamic Rerouting-2	[90]	2004	Providing Extra Link	Yes	Yes	Distance tag routing
DRGIN	Dynamic Rerouting GIN	[90]	2004	Increasing the number of network ports slightly	Yes	No	Distance, Destination tag routing
B-Network	Backward Network	[89]	1990	Providing back links	Yes	Yes	Distance routing
DR Network	Dynamic Rerouting Network	[102]	2014	Increasing the number of network ports slightly	No	No	Dynamic Rerouting
ILN	Improved logical Neighborhood network	[102]	2014	Completing inherent partial redundancy	Yes	Yes	Dynamic Rerouting
IEADM	Improved Enhanced Augmented data Manipulator	[102]	2014	Completing inherent partial redundancy	Yes	Yes	Dynamic Routing

Table A.3. Terminal Reliability of Gamma Interconnection Networks for 8×8 network size.

Network	TR (R_{SE}=0.9)								TR (R_{SE}=0.7)							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
GIN	0.7551	0.8381	0.8306	0.8381	0.7551	0.8381	0.8306	0.8381	0.3863	0.5370	0.5022	0.5370	0.3863	0.5370	0.5022	0.5370
EGIN	0.9263	0.9183	0.9279	0.9183	0.9263	0.9183	0.9279	0.9183	0.6680	0.6356	0.6869	0.6356	0.6680	0.6356	0.6869	0.6356
CGIN	0.9286	0.9211	0.9272	0.8985	0.8985	0.8985	0.9272	0.9211	0.7193	0.6845	0.7015	0.5833	0.5833	0.5833	0.7015	0.6845
MGIN	0.9280	0.9204	0.9136	0.8306	0.8985	0.8306	0.9136	0.9204	0.7120	0.6772	0.6529	0.5022	0.5833	0.5022	0.6529	0.6772
BGIN	0.9425	0.9425	0.9425	0.9425	0.9425	0.9425	0.9425	0.9425	0.6076	0.6076	0.6076	0.6076	0.6076	0.6076	0.6076	0.6076
ReGIN	0.9129	0.9272	0.9211	0.9061	0.8985	0.9272	0.9211	0.9272	0.6424	0.7015	0.6845	0.6181	0.5833	0.7015	0.6845	0.7015
Incomplete GIN	0.8358	0.9208	0.8358	0.9182	0.8371	0.9182	0.8371	0.9182	0.5035	0.6593	0.5035	0.6345	0.5159	0.6345	0.5035	0.6345
Incomplete CGIN	0.9263	0.9244	0.9279	0.9292	0.9268	0.9194	0.9268	0.9292	0.6680	0.6526	0.6869	0.7003	0.6803	0.6531	0.6803	0.7003
NBGIN	0.8851	0.8851	0.8851	0.8851	0.8851	0.8851	0.8851	0.8851	0.5710	0.5710	0.5710	0.5710	0.5710	0.5710	0.5710	0.5710
Modified BGIN	0.9258	0.9129	0.9286	0.9129	0.8985	0.9129	0.9286	0.9129	0.6838	0.6424	0.7193	0.6424	0.5833	0.6424	0.7193	0.6424
RIN-1	0.9812	0.9812	0.9812	0.9812	0.9812	0.9812	0.9812	0.9812	0.8029	0.8029	0.8029	0.8029	0.8029	0.8029	0.8029	0.8029
RIN-2	0.8670	0.8670	0.8670	0.8670	0.8670	0.8670	0.8670	0.8670	0.5574	0.5574	0.5574	0.5574	0.5574	0.5574	0.5574	0.5574
3DCGIN	0.8981	0.8966	0.8986	0.8966	0.8981	0.8966	0.8986	0.8966	0.6553	0.6386	0.6565	0.6386	0.6553	0.6386	0.6565	0.6386
3DGIN	0.9086	0.9086	0.9078	0.9058	0.8755	0.9058	0.9078	0.9078	0.6829	0.6829	0.6712	0.6481	0.5885	0.6481	0.6712	0.6712
4DGIN-1	0.8291	0.8291	0.8291	0.8291	0.8290	0.8290	0.8290	0.8290	0.5251	0.5251	0.5251	0.5251	0.5234	0.5234	0.5217	0.5217
4DGIN-2	0.8291	0.8291	0.8291	0.8291	0.8290	0.8290	0.8290	0.8290	0.5251	0.5251	0.5251	0.5251	0.5234	0.5234	0.5217	0.5217
CSMIN / CSGIN	0.8546	0.8546	0.8546	0.8546	0.8546	0.8546	0.8546	0.8546	0.5070	0.5070	0.5070	0.5070	0.5070	0.5070	0.5070	0.5070
CSMINMD	0.9851	0.9851	0.9851	0.9851	0.9851	0.9851	0.9851	0.9851	0.7102	0.7102	0.7102	0.7102	0.7102	0.7102	0.7102	0.7102
FCSMIN	0.8646	0.8646	0.8646	0.8646	0.8646	0.8646	0.8646	0.8646	0.5275	0.5275	0.5275	0.5275	0.5275	0.5275	0.5275	0.5275
PCGIN	0.8502	0.8646	0.8574	0.8574	0.8502	0.8574	0.8574	0.8646	0.4681	0.5275	0.4978	0.4978	0.4681	0.4978	0.4978	0.5275
FCGIN	0.8502	0.8502	0.8502	0.8502	0.8502	0.8502	0.8502	0.8502	0.4681	0.4681	0.4681	0.4681	0.4681	0.4681	0.4681	0.4681
EIADM	0.9235	0.9212	0.9015	0.9157	0.8987	0.9157	0.9015	0.9212	0.5301	0.5783	0.5517	0.5783	0.5301	0.5783	0.5517	0.5783
FTIN	0.8288	0.8288	0.8288	0.8288	0.8288	0.8288	0.8288	0.8288	0.5130	0.5130	0.5130	0.5130	0.5130	0.5130	0.5130	0.5130
MINGIN 1	0.8251	0.8251	0.8251	0.8251	0.8251	0.8251	0.8251	0.8251	0.4502	0.4502	0.4502	0.4502	0.4502	0.4502	0.4502	0.4502
MINGIN 2	0.8791	0.8791	0.8791	0.8791	0.8791	0.8791	0.8791	0.8791	0.5061	0.5061	0.5061	0.5061	0.5061	0.5061	0.5061	0.5061
DRGIN	0.7694	0.8306	0.9061	0.7551	0.8306	0.7551	0.9061	0.8306	0.4454	0.5022	0.6181	0.3863	0.5022	0.3863	0.6181	0.5022
B-Network	0.8579	0.8579	0.8579	0.8579	0.8579	0.8579	0.8579	0.8579	0.4656	0.4656	0.4656	0.4656	0.4656	0.4656	0.4656	0.4656
DR Network	0.7551	0.8381	0.8306	0.8381	0.7551	0.8381	0.8306	0.8381	0.3863	0.5370	0.5022	0.5370	0.3863	0.5370	0.5022	0.5370
ILN	0.9974	0.9974	0.9974	0.9974	-	-	-	-	0.8611	0.8611	0.8611	0.8611	-	-	-	-
IEADM	0.9085	0.9085	0.9085	0.9085	-	-	-	-	0.6244	0.6244	0.6244	0.6244	-	-	-	-

Table A.4. Terminal Reliability for R_{SE}=0.5, Broadcast Reliability and Network Reliability of different Gamma Networks for 8×8 network size.

Network	TR (R_{SE}=0.5)								BR for R_{SE}=			NR for R_{SE}=		
	0	1	2	3	4	5	6	7	0.9	0.7	0.5	0.9	0.7	0.5
GIN	0.1575	0.2756	0.2362	0.2756	0.1575	0.2756	0.2362	0.2756	0.5727	0.0923	0.0057	0.4953	0.0485	0.0012
EGIN	0.3091	0.2830	0.3321	0.2830	0.3091	0.2830	0.3321	0.2830	0.7166	0.2392	0.0301	0.5528	0.0823	0.0027
CGIN	0.4233	0.3839	0.3937	0.2756	0.2756	0.2756	0.3937	0.3839	0.6400	0.1680	0.0188	0.5535	0.0882	0.0040
MGIN	0.4134	0.3740	0.3544	0.2362	0.2756	0.2362	0.3544	0.3740	0.6400	0.1680	0.0188	0.4953	0.0485	0.0012
BGIN	0.2482	0.2482	0.2482	0.2482	0.2482	0.2482	0.2482	0.2482	0.6863	0.1948	0.0222	0.3381	0.0088	0.0000
ReGIN	0.3347	0.3937	0.3839	0.3150	0.2756	0.3937	0.3839	0.3937	0.5727	0.0923	0.0057	0.4953	0.0485	0.0012
Incomplete GIN	0.2116	0.3125	0.2116	0.2830	0.2264	0.2830	0.2264	0.2830	0.5762	0.0987	0.0047	0.2856	0.0027	0.0000
Incomplete CGIN	0.3091	0.2928	0.3321	0.3465	0.3281	0.3104	0.3281	0.3465	0.5295	0.0928	0.0066	0.2856	0.0027	0.0000
NBGIN	0.2700	0.2700	0.2700	0.2700	0.2700	0.2700	0.2700	0.2700	0.6976	0.2063	0.0291	0.3621	0.0204	0.0003
Modified BGIN	0.3642	0.3347	0.4233	0.3347	0.2756	0.3347	0.4233	0.3347	0.6400	0.1680	0.0188	0.4432	0.0266	0.0004
RIN-1	0.4440	0.4440	0.4440	0.4440	0.4440	0.4440	0.4440	0.4440	0.7328	0.2949	0.0681	0.3901	0.0336	0.0007
RIN-2	0.2279	0.2279	0.2279	0.2279	0.2279	0.2279	0.2279	0.2279	0.7330	0.3005	0.0770	0.6557	0.2303	0.0471
3DCGIN	0.3564	0.3320	0.3525	0.3320	0.3564	0.3320	0.3525	0.3320	0.6576	0.1752	0.0187	0.3489	0.0061	0.0000
3DGIN	0.3924	0.3924	0.3713	0.3375	0.2908	0.3375	0.3713	0.3713	0.5958	0.1019	0.0066	0.5114	0.0818	0.0047
4DGIN-1	0.2686	0.2686	0.2686	0.2686	0.2637	0.2637	0.2588	0.2588	0.6259	0.2003	0.0391	0.4725	0.0759	0.0054
4DGIN-2	0.2686	0.2686	0.2686	0.2686	0.2637	0.2637	0.2588	0.2588	0.6259	0.2003	0.0391	0.4725	0.0759	0.0054
CSMIN / CSGIN	0.2143	0.2143	0.2143	0.2143	0.2143	0.2143	0.2143	0.2143	0.6976	0.2063	0.0291	0.4576	0.0450	0.0014
CSMINMD	0.3211	0.3211	0.3211	0.3211	0.3211	0.3211	0.3211	0.3211	0.6761	0.1195	0.0079	0.3794	0.0239	0.0004
FCSMIN	0.2315	0.2315	0.2315	0.2315	0.2315	0.2315	0.2315	0.2315	0.6417	0.1208	0.0083	0.4631	0.0354	0.0006
PCGIN	0.1736	0.2315	0.2025	0.2025	0.1736	0.2025	0.2025	0.2315	0.5759	0.1117	0.0093	0.3630	0.0201	0.0002
FCGIN	0.1736	0.1736	0.1736	0.1736	0.1736	0.1736	0.1736	0.1736	0.6153	0.1080	0.0091	0.2658	0.0029	0.0000
EIADM	0.2625	0.2562	0.2068	0.2160	0.1867	0.2160	0.2068	0.2562	0.5411	0.0552	0.0017	0.4027	0.0131	0.0001
FTIN	0.2352	0.2352	0.2352	0.2352	0.2352	0.2352	0.2352	0.2352	0.6259	0.2003	0.0391	0.4721	0.0738	0.0049
MINGIN 1	0.1701	0.1701	0.1701	0.1701	0.1701	0.1701	0.1701	0.1701	0.6124	0.1031	0.0061	0.4510	0.0353	0.0007
MINGIN 2	0.1849	0.1849	0.1849	0.1849	0.1849	0.1849	0.1849	0.1849	0.5727	0.0923	0.0057	0.4510	0.0353	0.0007
DRGIN	0.2165	0.2362	0.3150	0.1575	0.3453	0.1575	0.3150	0.2362	0.5727	0.0923	0.0057	0.4432	0.0266	0.0004
B-Network	0.1722	0.1722	0.1722	0.1722	0.1722	0.1722	0.1722	0.1722	0.4890	0.0431	0.0013	0.2035	0.0046	0.0000
DR Network	0.1575	0.2756	0.2362	0.2756	0.1575	0.2756	0.2362	0.2756	0.5727	0.0923	0.0057	0.4953	0.0485	0.0012
ILN	0.4189	0.4189	0.4189	0.4189	-	-	-	-	0.9974	0.8611	0.4189	0.9974	0.8611	0.4189
IEADM	0.2837	0.2837	0.2837	0.2837	-	-	-	-	0.8587	0.3435	0.0612	0.7526	0.1191	0.0037

Table A.5. TR, BR and NR of different Gamma Networks as a function of Network Size ‘N’.

Network	TR as a function of network size N=			BR as a function of network size N=			NR as a function of network size N=		
	16	**64**	**1024**	**16**	**64**	**1024**	**16**	**64**	**1024**
GIN	0.6796	0.5504	0.3611	0.2952	0.0043	0	0.1861	0.0000	0
EGIN	0.9057	0.8553	0.7005	0.4398	0.0000	0	0.2678	0.0001	0.0000
GIN-	0.9587	0.8881	0.7009	0.8121	0.0912	0	0.6303	0.0467	0
CGIN	0.7278	0.5393	0.2711	0.2952	0.0043	0	0.2536	0.0000	0.0000
MGIN	0.7278	0.5393	0.2711	0.2952	0.0043	0	0.1861	0.0000	0
BGIN	0.9150	0.8624	0.7661	0.5130	0.0793	0.0000	0.0755	0.0000	0
ReGIN	0.8637	0.7758	0.5824	0.2952	0.0043	0	0.1861	0.0000	0
Incomplete GIN	0.7939	0.7185	0.5440	0.3843	0.0110	0	0.0677	0.0000	0
Incomplete CGIN	0.9212	0.8830	0.7405	0.5011	0.0279	0.0000	0.0677	0.0000	0
NBGIN	0.8264	0.7465	0.5640	0.3657	0.0155	0.0000	0.1046	0.0000	0
Modified BGIN	0.8637	0.7758	0.5824	0.2952	0.0043	0	0.1366	0.0000	0
RIN-1	0.8568	0.8271	0.7126	0.4117	0.0313	0	0.1347	0.0000	0.0000
RIN-2	0.9030	0.8830	0.7848	0.4119	0.0313	0	0.2971	0.0002	0.0000
3DCGIN	0.8161	0.7273	0.5409	0.3033	0.0045	0	0.0649	0.0000	0
3DGIN	0.8663	0.8277	0.6905	0.4961	0.0945	0.0000	0.2276	0.0000	0
4DGIN-1	0.8262	0.8103	0.7226	0.4300	0.0453	0.0000	0.2042	0.0000	0.0000
4DGIN-2	0.8262	0.8103	0.7226	0.4300	0.0453	0.0000	0.2042	0.0000	0.0000
CSMIN / CSGIN	0.8264	0.7465	0.5640	0.3657	0.0155	0.0000	0.2015	0.0000	0.0000
CSMINMD	0.9208	0.8434	0.6473	0.2071	0.0023	0	0.1386	0.0000	0.0000
FCSMIN	0.7133	0.5778	0.3791	0.2972	0.0051	0	0.1278	0.0000	0
PCGIN	0.6716	0.5440	0.3569	0.4141	0.0330	0.0000	0.1061	0.0000	0.0000
FCGIN	0.8257	0.7359	0.5473	0.0630	0.0046	0	0.0341	0.0000	0
EIADM	0.7221	0.4656	0.1615	0.2320	0.0000	0	0.0995	0.0000	0
FTIN	0.8088	0.0141	0	0.3947	0.0008	0	0.2055	0.0000	0.0000
MINGIN 1	0.8405	0.7511	0.5603	0.2858	0.0001	0	0.1543	0.0000	0
MINGIN 2	0.8640	0.8346	0.7787	0.2952	0.0043	0	0.1543	0.0000	0

(Table A.5) cont.....

DRGIN	0.8987	0.8534	0.7084	0.2952	0.0043	0	0.1366	0.0000	0
B-Network	0.8095	0.7161	0.5278	0.1822	0.0015	0.0000	0.0178	0.0000	0.0000
DR Network	0.6796	0.5504	0.3611	0.2952	0.0043	0	0.1861	0.0000	0
ILN	0.0548	0	0	0.0548	0	0	0.0548	0	0
IEADM	0.9817	0.9797	0.9758	0.6286	0.0464	0	0.0021	0.0000	0

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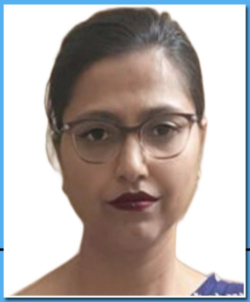
SUBJECT INDEX

Shilpa Gupta



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